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Pulsed Power and Load-Pull Measurements for Microwave Transistors

Sivalingam Somasundaram Meena
University of South Florida

Pulsed Power and Load-Pull Measurements for Microwave Transistors

by

Sivalingam Somasundaram Meena

A thesis submitted in partial fulfillment
of the requirements for the degree of
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Co-Major Professor: Lawrence P. Dunleavy, Ph.D.
Co-Major Professor: Charles Passant Baylis II, Ph.D.
Jing Wang, Ph.D.

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DEDICATION

MATHA, PITHA, GURU, DEIVAM

[MOTHER, FATHER, TEACHER, GOD]

As the famous saying in Sanskrit dictates this thesis is dedicated to my wonderful parents and teachers who have raised me to be the person I am today. You have always stood beside me in my success, failure and hard times. Thank you for the unconditional love, guidance, courage and support that you have always given me, helping me to overcome failure and instilling in me the courage to believe that I am capable of doing anything that I put my mind to. Thank you for everything.

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ABSTRACT

A novel method is shown for fitting and/or validating electro-thermal models using pulsed I(V) measurements and pulsed I(V) simulations demonstrated using modifications of an available non-linear model for an LDMOS (Laterally Diffused Metal Oxide Semiconductor) device. After extracting the thermal time constant, good agreement is achieved between measured and simulated pulsed I(V) results under a wide range of different pulse conditions including DC, very short (<0.1%) duty cycles, and varied pulse widths between these extremes. A pulsed RF load-pull test bench was also assembled and demonstrated for a VDMOS (Vertically Diffused Metal Oxide Semiconductor) and an LDMOS power transistor. The basic technique should also be useful for GaAs and GaN transistors with suitable consideration for the complexity added by trapping mechanisms present in those types of transistors.

CHAPTER 1

INTRODUCTION

The market demand for wireless devices for commercial and military continues to grow and with it the market for high power transistors for applications such as phased-array Antennas, Base Stations, Radars etc.,. The transistors that fill these requirements include Si-LDMOS GaAs pHEMTs and GaN-based transistors as they offer High Cut-Off frequencies and high frequencies of oscillation [1]. Since the overall power required from such transistor amplifiers used in microwave transmitters can be large, and unless the DC to RF conversion efficiency is 100% a considerable amount of power is dissipated in the substrate, which causes self-heating [2]. Sometimes self-heating effects are so significant that the devices can only operate or be tested safely under pulsed conditions. For example, on-wafer probing measurements of more than 500µm gate-width devices can be difficult in CW operation due to their insufficient heat sink [3]. So studying power devices under pulsed condition allows one to study the device under different temperatures of operation to enable a better understanding of the thermal behavior [1].

Also some applications, such as radar, require amplifiers that are designed to work optimally for a specific type of pulsed RF input. Combining pulsed RF and pulsed DC in a general load-pull system can allow self-heating to be avoided or controlled during device measurement. Therefore by performing pulsed- load- pull one can measure heat free characteristics of power devices, and obtain a better understanding of heat

dissipation mechanism and in turn build a robust model that integrates thermal effects. Well controlled pulsed RF and I(V) testing can also enable better insight into the influence of the thermal effects and how to model them.

Such insight and modeling may, for example, be used to minimize RF carrier phase shift within the output RF pulse of a power amplifier used for coherent radar application. Or it may help in the investigation of power amplifiers used in time-division multiple-accesses (TDMA) applications.

The literature shows that static DCIV measurements without separate electro-thermal (self heating) modeling can lead to inaccurate RF models [4], [5]. The aim of this thesis is to explore and implement pulsed measurements for characterizing transistors. In pulsed measurements, depending on the pulse width and duty cycle, the slow processes like self-heating and trapping do not have time to occur; thus it is safe to say that it is similar to the RF operation of the transistor [6]. Chapter 2 explains a pulsed simulation approach for prediction of duty-cycle dependent thermal effects in transistors. Also a novel method is shown for fitting and/or validating electro-thermal models using pulsed measurements and pulsed simulations. A commercial LDMOS (Laterally Diffused Metal Oxide Semiconductor) transistor is used to demonstrate the new methods. After fitting the curve and obtaining the thermal time, a very good agreement is achieved between measured and simulated pulsed I(V) results under a wide range of different pulse conditions including DC, very short (<0.1%) duty cycles, and settings between these extremes. A three pole electro-thermal equivalent circuit model was shown to get a better fit. In Chapter 3 a detailed experimental analysis was conducted of the pulsed

load-pull system developed as part of this research. Comparisons are made of the use of thermal and diode sensors for variable duty cycle pulsed RF measurements.

Chapter 4 describes a pulsed load-pull system that was constructed using a thermal sensor. This system had a pulsed RF input and a static bias. The advantage of using pulsed power over (continuous wave) CW was seen in the form of higher gain and efficiency. The pulsed system proved to mitigate the self heating in the VDMOS (Vertically Diffused Metal Oxide Semiconductor) transistors used; it also keeps the device operation safer when compared to CW power.

Chapter 5 shows pulsed load-pull measurements done for a LDMOS transistor and the same results were observed. Also the time domain representation of the pulsed signal at the various ports of the pulsed load-pull system is shown using an oscilloscope.

CHAPTER 2

NON-LINEAR MODEL SIMULATION OF PULSED I(V) BEHAVIOR

In any modeling process, in order for the model to predict the device operation, the measurements taken as the basis for model extraction should allow thermal and trapping conditions to occur in the same manner in which they occur at RF/microwave frequencies [7]. In high frequency operation the current and voltage of the device are altered so fast that slow processes like self-heating and trapping, which depend upon the steady state voltage and current, are not able to respond to the quick RF waveform [8]. So in Pulsed I(V) a steady state, also called quiescent, current and voltage is set for long enough for the steady state conditions to be reached. Then a pulse is applied from this quiescent bias point to different regions in the I(V) plane. If the pulse length is short enough, the thermal and trapping effects will not have time to change and thus a measurement is made with thermal and trapping effects that reflect only from the quiescent bias point condition. These measurements are sometimes called isothermal, where thermal conditions are held to a constant, and isodynamic [7], where both thermal and trapping states are held constant. For pulsed I(V) testing performed for this thesis two different commercial systems were employed variously. One is an Auriga 4750 and the other was a Dyanamic I(V) Analyzer (Diva) 265, formerly manufactured by Accent Opto-Electronics.

In this chapter it is shown that suitably modified transistor models, such as the Motorola Electro-Thermal (MET) for LDMOS [9], can be used along with pulsed simulations to accurately predict duty cycle dependent self heating effects [10]. Pulsed I(V) measurement analysis of a number of different candidate demonstration devices was used to select a device which had significant self-heating for larger pulse widths.

2.1. Introduction to Thermal Modeling

In a LDMOS model like a MET model as shown in this chapter has a dependence on channel temperature which is represented by some of the model parameters [11], while using a thermal "circuit" to calculate the channel temperature from the power dissipated in the FET (the following development can also be performed for bipolar devices with appropriate changes in terminology). Figure.2.1 displays the thermal circuit that is used to calculate the channel temperature as a function of frequency. In this circuit, R_{TH} is the thermal resistance, C_{TH} is the thermal capacitance, T_a is the ambient temperature (the temperature of the back side of the device), P_d is the power dissipated in the channel of the FET, and T_c is the channel temperature. In the thermal circuit analogy, temperature is analyzed as voltage and power as current. The thermal sub-circuit is very effective because it allows thermal calculations to be performed by a circuit analysis software tool. As given by (2.1)

$$P_d = V_{DS}I_D \qquad (2.1)$$

where V_{DS} is the drain-source voltage and I_D is the drain current.

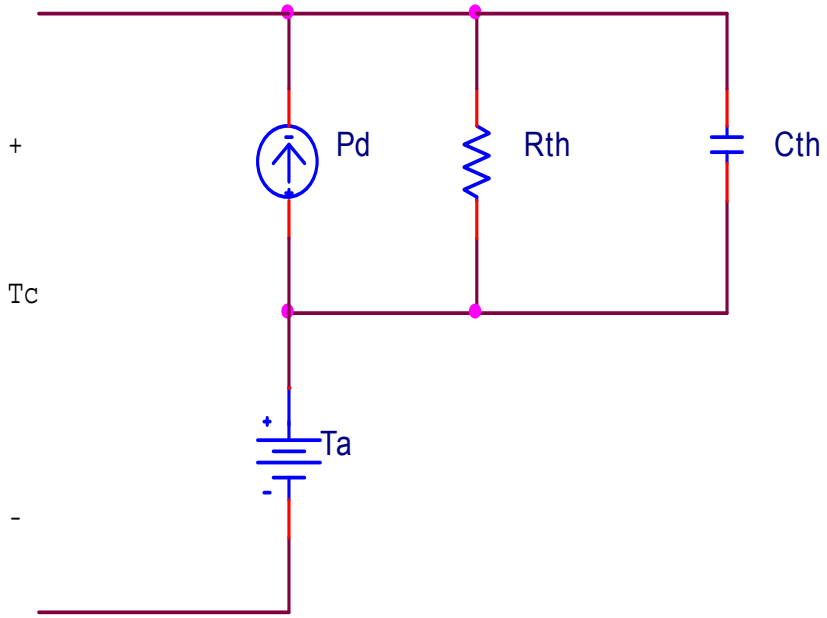


Figure.2.1. Thermal Sub-Circuit used in Electro-Thermal Models [7]

2.2. Pulsed I(V) Simulation

An Agilent Advanced Design System (ADS) simulation was set-up to predict the duty cycle dependent self-heating. In a traditional DC I(V) simulation set-up the only way to see the pulsed I(V) results is to set the thermal resistance R_{TH} to a very low value; however by using the pulsed I(V) simulation set-ups developed through this work, prediction of duty cycle dependent thermal effects in transistors is possible. Also a novel method is shown for extracting the thermal time constant ($\tau_{th} = 1/R_{th}C_{th}$ using the pulsed simulation technique) using curve fitting. Using this method thermal capacitance (C_{th}) can be determined provide thermal resistance R_{TH} is determined from an independent method [11] (See Appendix B). A commercial LDMOS device is used to demonstrate the new methods. After getting the thermal time constant, comparisons are made

between measured and simulated pulsed I(V) results under a wide range of different pulse conditions ranging from DC to very short (<0.1%) duty cycles and everywhere in-between.

There are a significant number of publications on nonlinear transistor modeling that include self-heating effects in MOSFETs and MESFET transistors [12]-[15]. A relatively smaller focus has been paid in the literature to the validation of duty-cycle dependent modeling and related electro-thermal model extractions. It has been shown that low duty-cycle pulsed I (V) measurement can be used to characterize thermal effects of transistors [12]-[16]. In a simple single pole electro thermal model there is a need to characterize both the thermal resistance and the thermal capacitance as shown in Figure.2.1. Multi-pole models require the extraction of several thermal resistances and capacitances [10], [17].

It is demonstrated in this work that such a simulation can be performed using the transient domain capability within Agilent Technologies ADS (ver. 2006A). This simulation capability is used in combination with variable duty cycle pulsed I(V) measurements to extract an electro thermal model valid for any duty cycle between short pulse (e.g. <0.01% duty cycle) and static conditions (100% duty cycle). An LDMOS power transistor is used to demonstrate the methods developed for extraction and validation of models that remain valid under varied bias current duty-cycles. Figure.2.2 compares pulsed and static I(V) for a 10 W Freescale LDMOS device (MRF281Z) for static and different pulsed condition. From Figure.2.2 and Figure.2.3 the self-heating can be clearly observed in the static I(V) data. Both static and pulsed measurements were made on the MRF281Z using Auriga's AU4750 Pulsed I(V)/RF system as well, since this

system allowed more flexible control of the measurement process. The AU4750 set-up is capable of producing pulse width (W) as small as 0.2 µs and pulse separation (S) was kept at 1 ms. Throughout the experiment the pulse separation was held at 1 ms and the pulse width was changed to change the duty cycle (D). In this case duty cycle is given by

$$D = \frac{W}{W + S} \qquad (2.2)$$

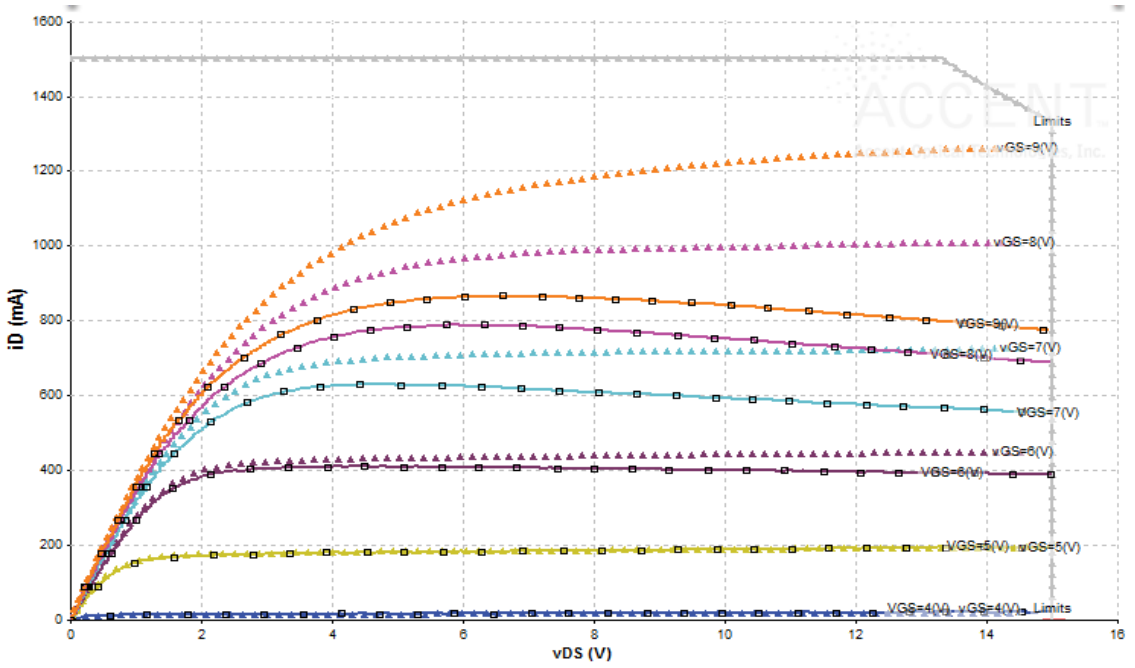


Figure.2.2. Comparison Between DC and Pulsed I(V) (Pulse Profile: W = 0.5 µs and S = 5ms), Q Point V_{ds} 15V and V_{gs} 3.5V [Pulsed Dotted Lines and Static Solid Lines]

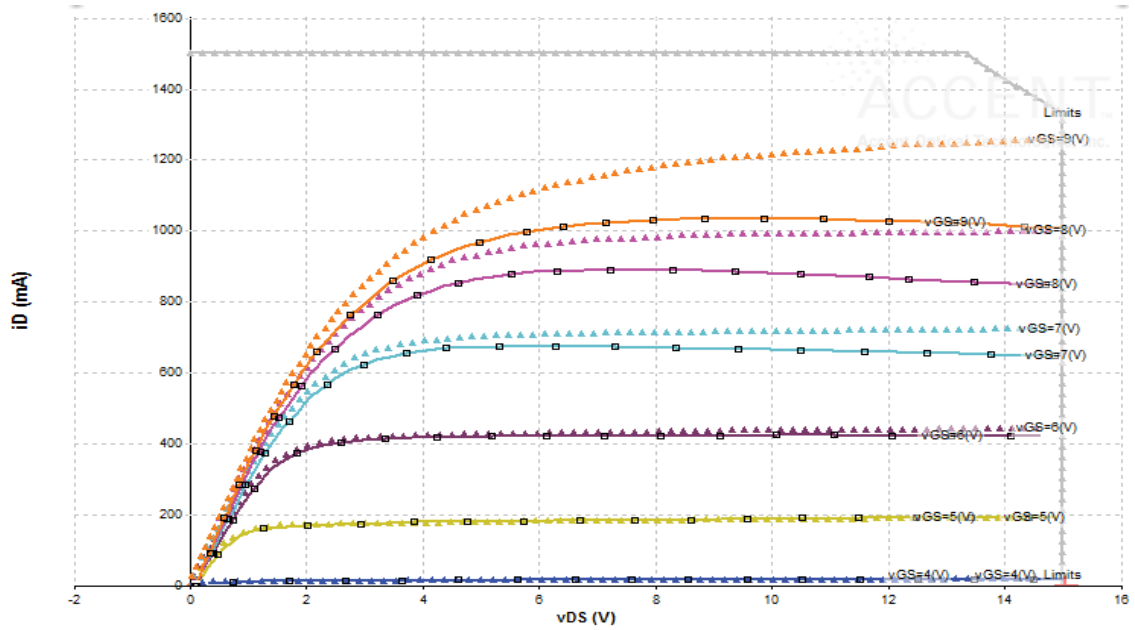


Figure.2.3. Comparison Between Different *W* (Pulse Profile: *W* 1 µs and *S* 5ms [Dotted Lines]; Pulse Profile: *W* = 1000 µs and *S* = 5ms [Solid Lines]), Q Point was V_{ds} 15V and V_{gs} 3.5V

Figure.2.4 explains the pulse waveform generation terminology (this data was taken with a DIVA D265 pulsed I(V) test system). Testing was done for *W* between 0.2 µs and 1000 µs, corresponding to duty cycles between 0.02 and 50%. Static, or 100% duty cycle DCIV was also tested.

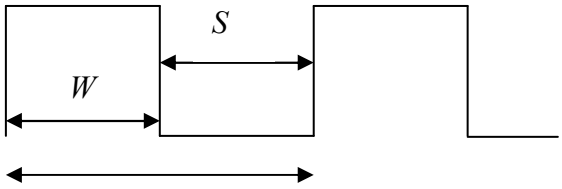


Figure.2.4. Important Aspects of Pulse Waveform as Used in The Pulsed I(V) Measurements

2.3. Measurements and Simulation

Both static and pulsed I(V) were measured at room temperature. For the pulsed I(V) measurements the quiescent bias point was held constant to keep the bias-dependent self heating the same. Two types of measurements were made for the present work:

1) Static I(V) measurement
2) Pulsed I(V) measurements with different W and quiescent point at V_{ds} 15 V and V_{gs} 3.5 V (I_{dq} ~0 corresponding to a Class B bias).

Both the measurements were done up to V_{ds} 14 V and V_{gs} 8 V. Figure.2.5 shows the comparison between static and pulsed measurement for a pulse width of 0.2 µs (which can be considered an isothermal measurement)

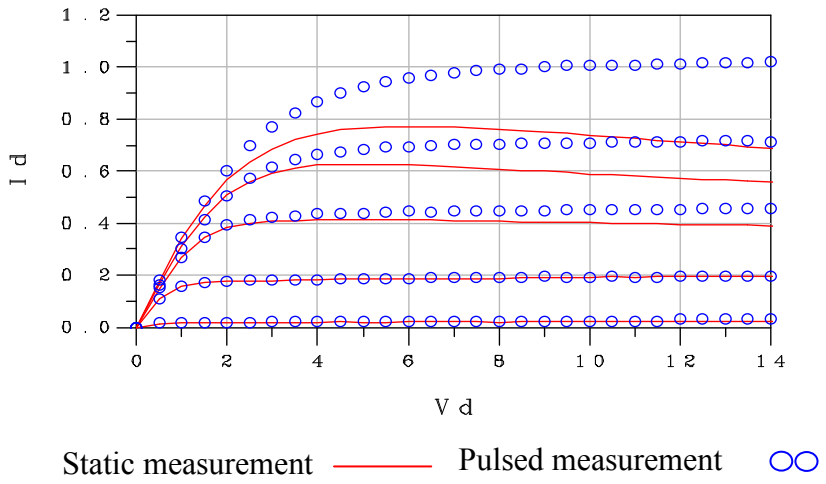


Figure.2.5. Static I(V) Measurement Vs Pulse I(V) Measurement (Pulse Profile: W =0.2 µs and S = 1ms, Q Point V_g = 3.5 and V_d = 15V). These Measurements were made with an Auriga AU4750 Test System.

The next figure shows a comparison between static I(V) measurements and pulsed I(V) measurements with W = 200 µs.

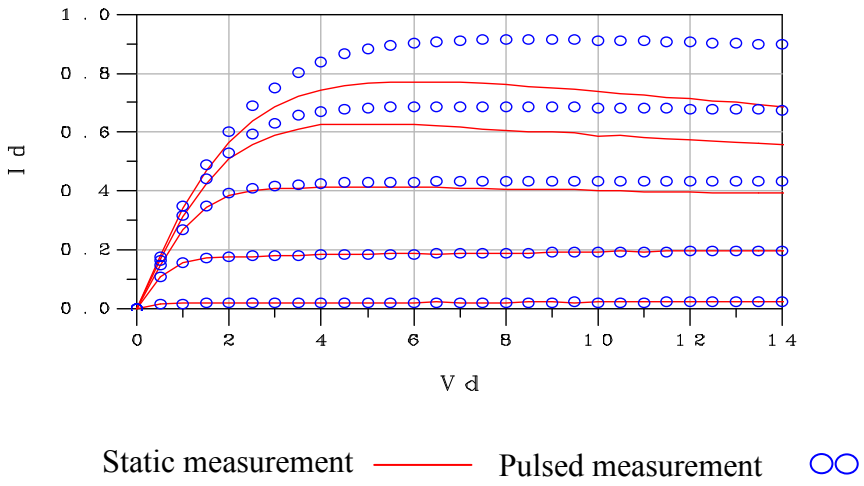


Figure.2.6. Static I(V) Measurement Vs Pulsed I(V) Measurement (Pulse Profile: Pulse Width 200 µs and Pulse Separation 1ms, Q Point V_g = 3.5 and V_d = 15V)

By comparing Figure.2.5 with Figure.2.6 it can be noted that as the W is increased, the self-heating increases and thus the drain current decreases. For long enough duty cycles, the pulsed I(V) results converge to the static case. If drain current I_d is measured for different W keeping the other constraints (S, quiescent point, temperature) constant , the resulting data can be used in combination with the pulsed I(V) simulations, explained below, to extract R_{TH} and C_{TH} of the device by fitting the simulation results to the measured data. For this work the R_{th} value of the model had already been determined for the device, by using methods consistent with [11] (See Appendix B).

The ADS schematic for the static simulation is shown in Figure.2.7.

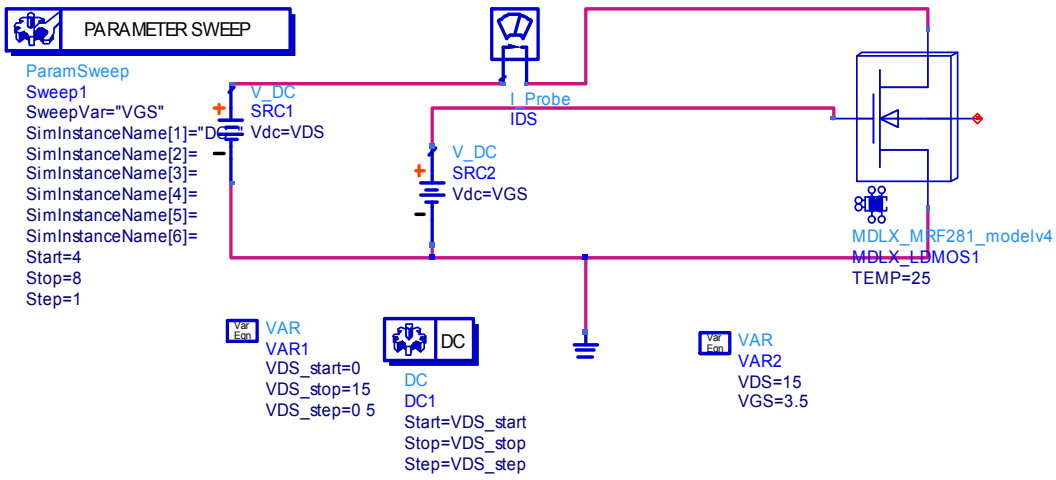


Figure.2.7. Static I(V) Simulation Schematic

In this work, a simulation method was established also for generating simulated pulsed I(V) curves. The pulsed voltage source used within Agilent ADS to generate the pulses is shown in Figure.2.8. By doing this type of simulation the current can be calculated for different *W* values These simulations can be compared with the measured pulsed I(V) curves, and the thermal model can then be adjusted for best fit between the measured and simulated transient current data sets.

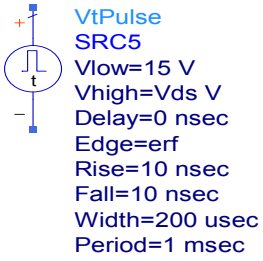


Figure.2.8. Pulsed Voltage Source Used in Pulsed I(V) Simulation

In Figure.2.8 Vlow represents the quiescent point for the drain of the device and Vhigh is the voltage when the pulse is turned ON (this value is set to be swept over a range covering the x-axis of the desired pulsed I(V)-Curve). Width is given by *W* and Period is the time period.

2.4. τ_{th} and/or C_{th} Extraction

Figure.2.9 shows the more complete schematics used in ADS to perform pulsed I(V) simulations. The simulation must be constructed such that I_d is sampled in a consistent way for all pulse widths and in a manner that is consistent with the sampling used on the bench as set-up but the Auriga 4750 acquisition aperture settings. By doing this type of simulation the current can be calculated for different values of *W*. These simulations can be compared with the measured pulsed I(V) curves, and the thermal model can then be adjusted for the best fit between the measured and simulated transient current data sets.

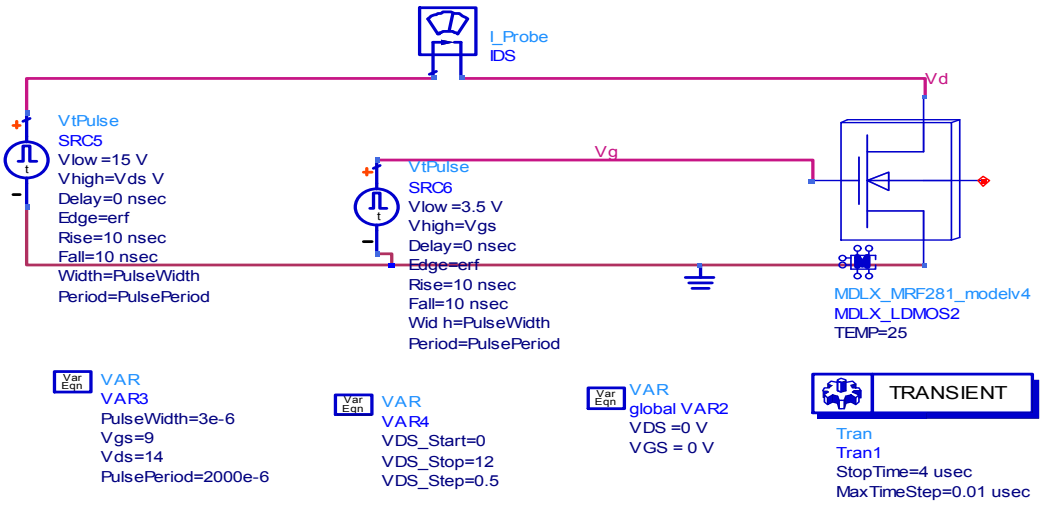


Figure.2.9. Pulsed I(V) Simulation Schematics

Thermal time constant (τ_{th}) extraction has been discussed in the literature [16], [18]. The methods discussed by previous papers are indirect and require an additional measurement step to measure the transient current I_d at different pulse conditions. The present work uses pulsed I(V) measurements directly. Transient simulation of pulsed I(V) is used to plot I_d for a particular V_{ds} and V_{gs}.

For this example the I(V) curve corresponding to the highest gate voltage was chosen so maximum self heating can be seen, as shown in Figures.2.10 and 2.11. Figure.2.10 shows the comparison between measured and simulated static I(V) curves using the previously developed model. Figure.2.11 shows the transient current value obtained by performing pulsed I(V) measurements (blue circles) and then selecting the current value corresponding to V_{ds}=14V, V_{gs} =8V. The measured I_d was obtained in this way from pulsed I(V) measurement at different P_W values (0.2 µs, 0.5 µs , 2 µs, 5 µs, 20 µs, 50 µs, 200 µs, 500 µs and 1000 µs). The simulation was done for a W=1100 µs so a continuous I_d curve is obtained which can be compared with the measurements at different pulse width. The thermal time constant is given by τ_{Th}. The blue dots in the Figure.2.9 represent the I_d measured at different pulse widths.

$$\tau_{Th} = R_{TH} * C_{TH} \qquad (2.3)$$

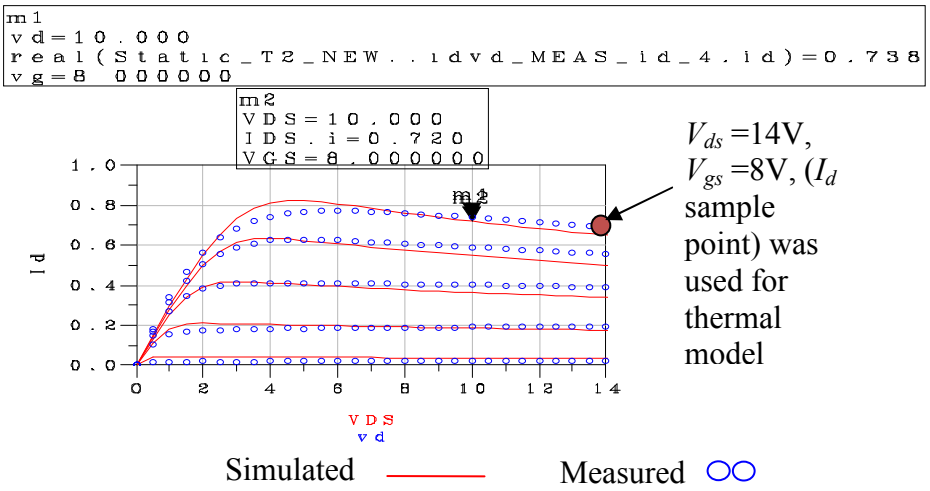


Figure.2.10. Static Measurement Vs Static Simulation with R_{TH} =3.2. For the ADS Simulation a Standard DCIV Schematic (Not Shown) was Used Along with the same Non-linear Model from Figure 2.9

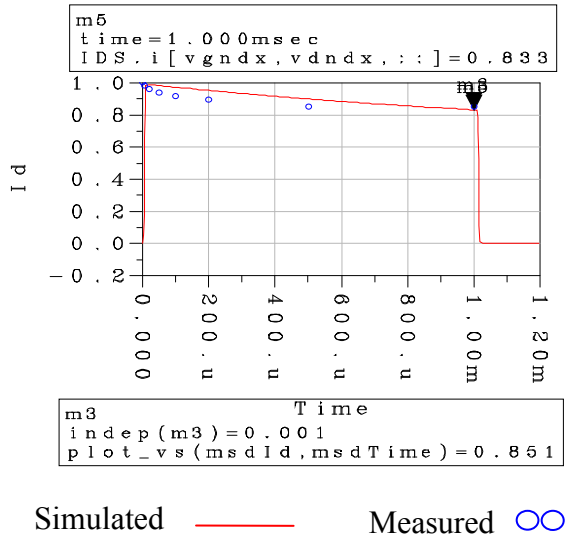


Figure.2.11. Comparison Between I_d Measured and Simulated At V_d = 14 V and V_g = 8 V (After τ_{Th} Extraction). The Schematic of Figure.2.9 was used to Produce Simulated Results

Using the simulation, the parameters of τ_{Hh} (or fitting thermal capacitance, $C_{TH,}$ with R_{TH} determined independently as mentioned above,) were extracted using a single pole thermal equivalent circuit to obtain a fit as shown in Figure.2.11. Before the fitting τ_{TH} was 0.1 ms (a guess value), after the fitting was found to be 2.4 ms.

2.5. Comparison Between Auriga and Transient Measurements

One other important method to predict the thermal time constant of a transistor is the transient measurement as given in [16]. The set-up for the transient measurement is shown in Figure 2.12.

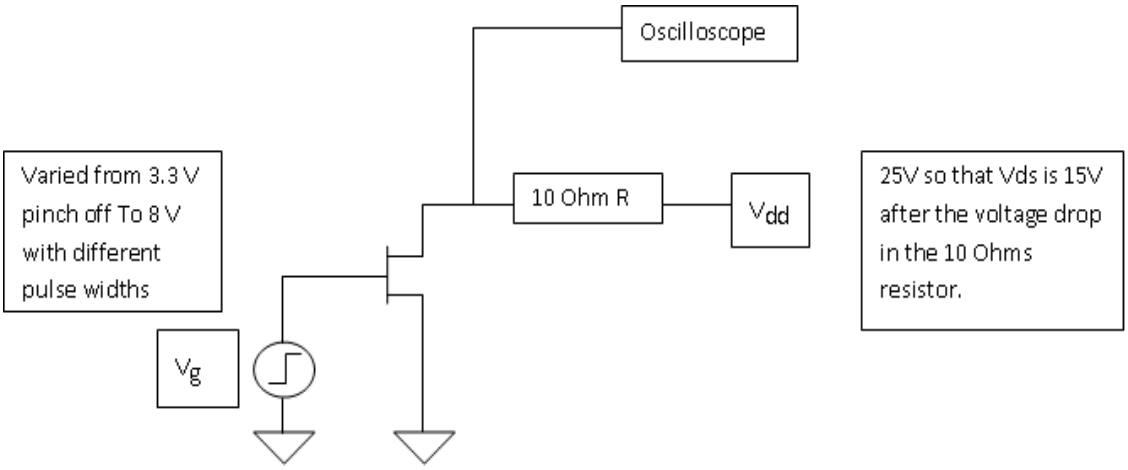


Figure.2.12. Transient Set-up [16]

From the above set-up it can be observed that the V_{dd} and V_g are kept at 8 V and 14 V, respectively, after accounting for the resistance of the 10 Ohm resistor and the cables resistance. With this set-up the current I_d obtained from transient measurement is

essentially from the same voltage conditions as in Figure.2.11. In the set-up shown in the above figure V_g is generated by using the digital delay generator (whose pulse width can be varied), V_{dd} is the constant voltage supply given by a power supply.

The initial value of the gate voltage is chosen below the threshold voltage of the device. With the gate voltage at this value (3.3V), no current is being conducted through the drain of the FET, so no voltage is dropped across the resistor. The initial value of the drain voltage $V_d(t) = V_{dd}$. The gate voltage is then stepped to a value that causes significant bias current (8V) to be conducted (and thus significant self-heating to occur). Current begins to flow through the drain and also the resistor, causing the voltage across the resistor to increase. The drain voltage thus decreases (for a fixed V_{dd}). However, as the device begins to heat up, the current decreases, causing the voltage drop across the resistor to decrease and the drain voltage V_d (t) to increase. Since at different pulse width the device has different self-heating, by changing the pulse width of the digital delay generator (it is possible) to obtain a transient I_d curve as shown in Figure 2.11 which can be compared with other pulsed I(V) measurements as done here. (NOTE: It should be noted that I_d does not occur at a fixed value of V_d unless the devise is in the saturation region. Since the transient measurement curve matches well with the Auriga's sampled I_d point it is a reasonable approximation). The current I_d was measured using the formula

$$Id = \frac{Vdd - Vd(t)}{R} \qquad (2.4)$$

Where

1) V_{dd} is 25V
2) V_d (t) is obtained from the oscilloscope measurements
3) R is 10 Ohms resistor.

The devices were measured using Transient method and Auriga system and a comparison is shown between the three measurements in Table.2.1

Table.2.1 I_d comparison using different measurement systems and simulation techniques

Time Pulse Width W (S)	*Transient measurements I_d (A)*	*Auriga I_d (A)*	*Simulation I_d (A)*
2.00E-07	0.96	0.978	0.983
1.00E-05	0.92	0.927	0.96
5.00E-05	0.87	0.878	0.896
1.00E-04	0.84	0.833	0.84
2.00E-04	0.8	0.804	0.78
5.00E-04	0.74	0.744	0.731
1.00E-03	0.7	0.706	0.7

The transient measurement for a W = 500 µs is shown in Figure.2.11. It can be observed that during the transient the V_d(t) increase as the I_d decreases. Since the transient measurement is somewhat more established [16], [18] the favorable comparison in Table.2.1 helps validate the methods presented here. (NOTE: This is only true if the device is in complete saturation at the time V_d(t) was measured, and I_d does not vary significantly with V_d(t) changes during the heating transient).

After some exploration it was found that a three pole electro-thermal equivalent circuit model provides for a more accurate fit to the transient data obtained. Figure.2.14 shows the three-pole model that was attached to 4th port of the non-linear MET model.

(To disable the built-in single pole model we set R_{TH} and C_{TH} to very small values within the MET model itself.).

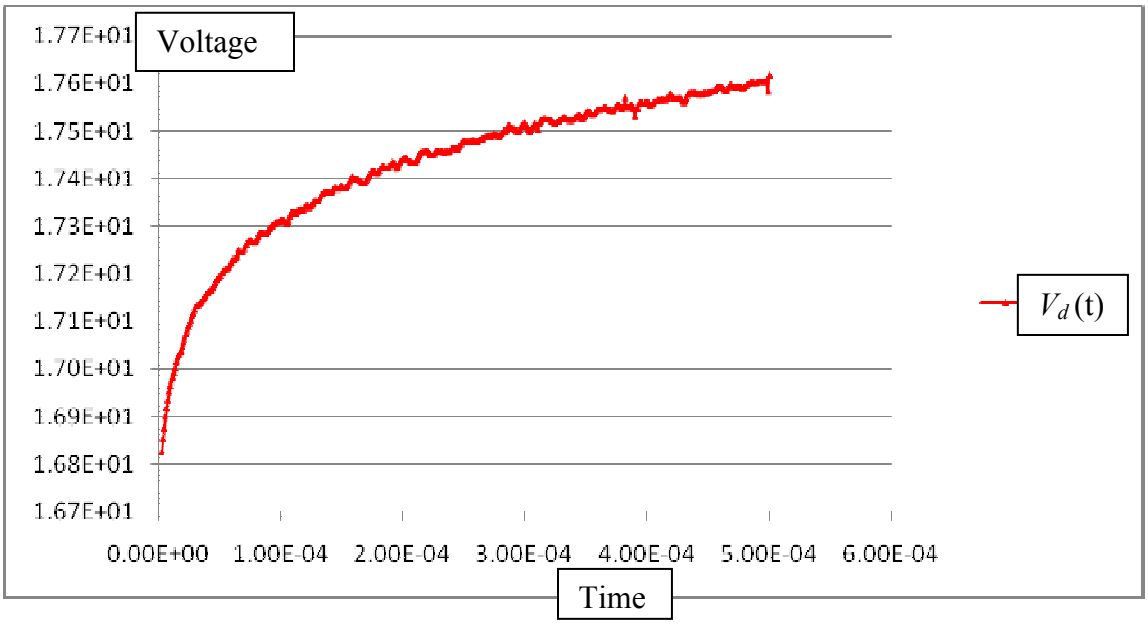


Figure.2.13. Transient Measurement for W = 500 µs

Figure.2.13. shows the simulated to measured transient current results after the three pole thermal circuit was fit and optimized until a best fit was obtained between the simulation and the measurement. Note that the sum of the resistances was restricted to add up to the original R_{TH} value of 3.2 ohms. Values for the R-C element values of this network were adjusted to get a best fit for the simulation to match the measurement for all duty cycles considered from the smallest W (0.2 µs) through the largest W (1ms) and all values in between. With this model it can be observed that the simulated curve has the same shape as the measurement curve.

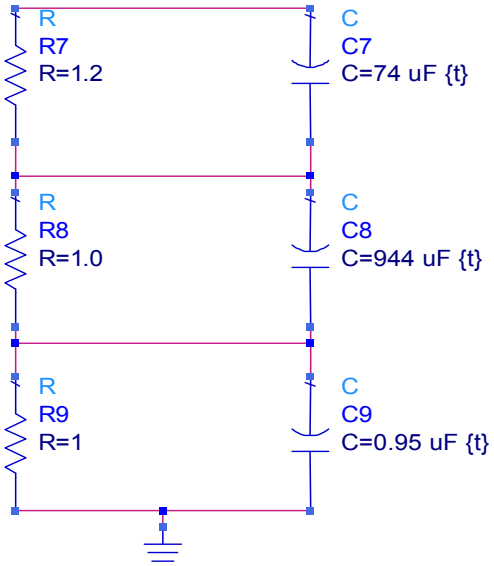
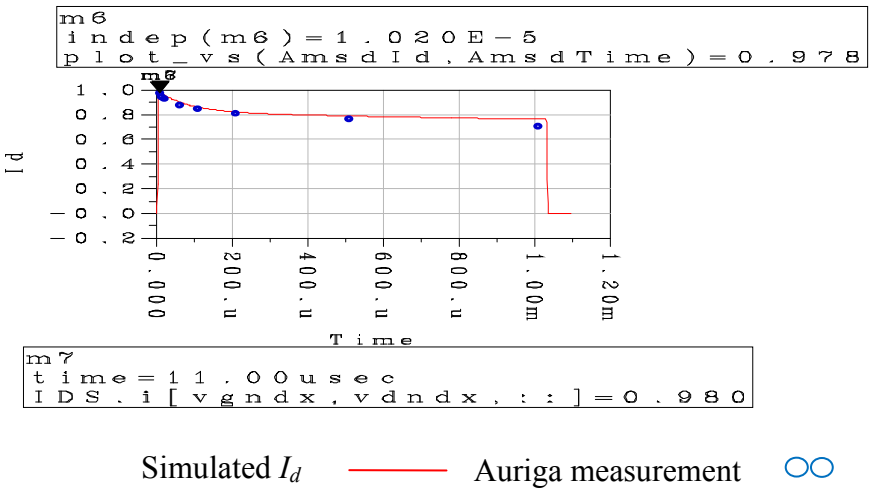


Figure.2.14. Three-pole Electro-thermal Model (Element values shown are the Final Optimized Values)

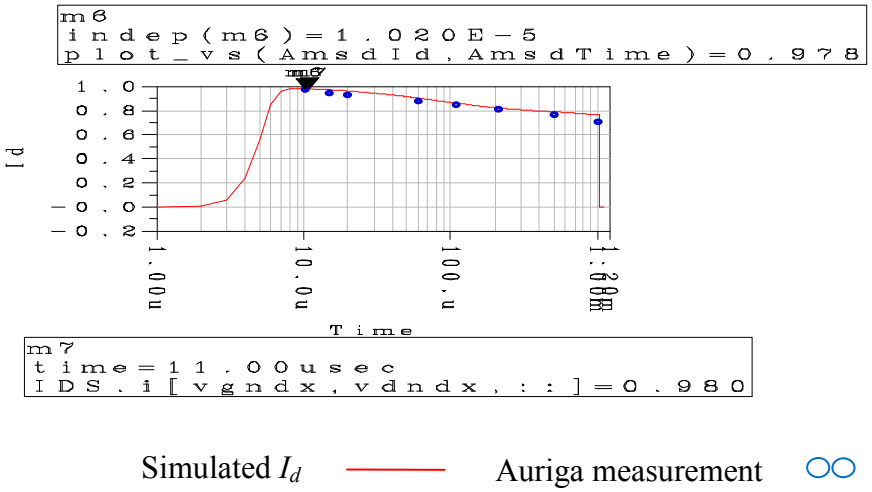
2.6. Measurement and Simulation Comparison

From Figure.2.16 it can be clearly seen that the MET model with multi-pole model is now able to predict the actual pulsed I(V) measurement very accurately which is very important in non-linear transistor design.

The electro-thermal circuit of Figure.2.14 was used along with the pre-existing MET model (extracted by Modelithics, Inc.) for the MRF281Z device and a good agreement was demonstrated between the simulation and the measurement for pulsed I(V) with different pulse widths as shown in Figure 2.16.



(a)



(b)

Figure.2.15. Comparison Between Id Measured and Simulated at V_d = 14 V and V_g = 8 V (After τ_{Th} Extraction) (a) in Linear Scale, (b) Log Scale. Measurements were taken with an Auriga AU4750

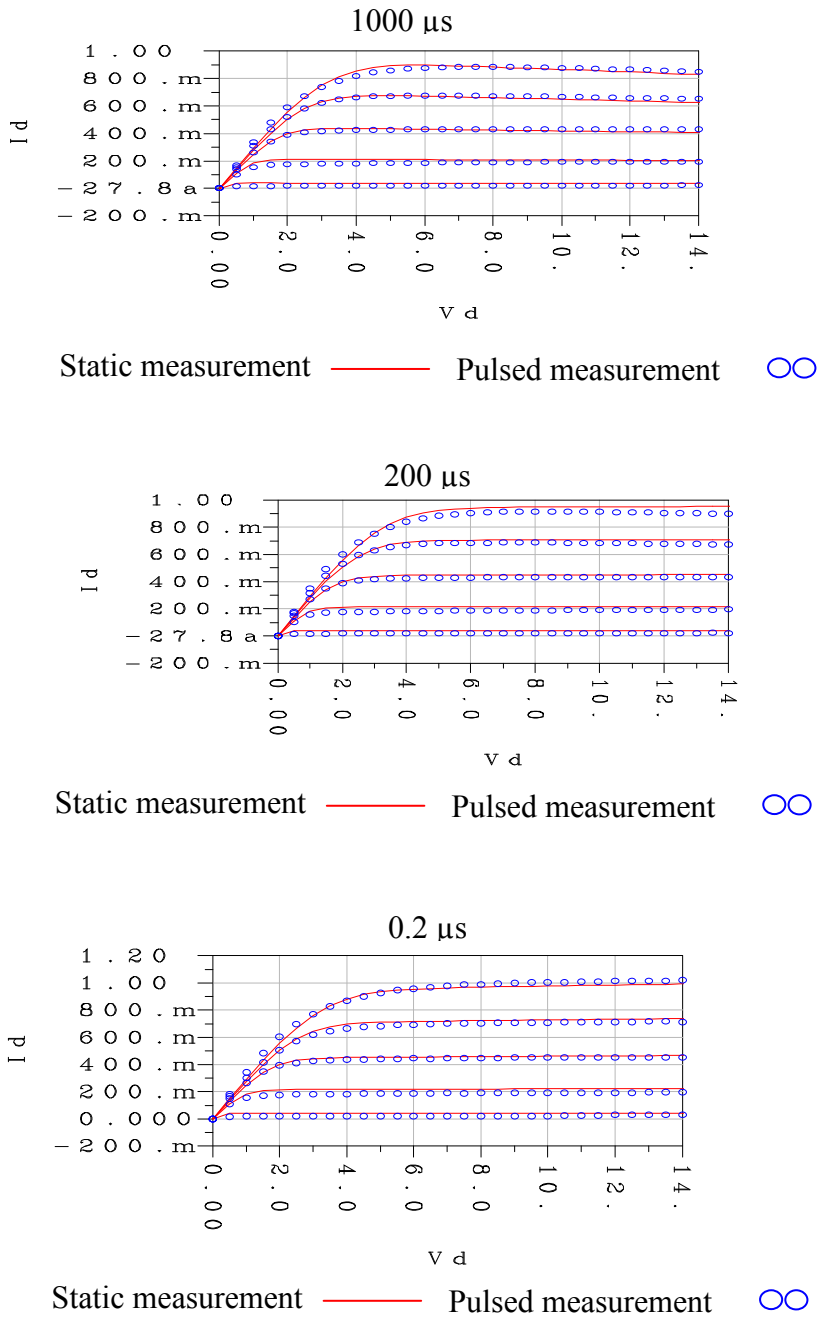


Figure.2.16. Comparison Between Pulsed I(V) Simulated and Measured After τ_{Th} Extraction for Varied Duty Cycles for a Single Pole Model

The Normalized Difference Unit (NDU) method as discussed in [11] has been used here to quantitatively compare the relative error between the simulation and measurement for various pulse widths as shown in Table.2.2

Table.2.2. NDU for Different *W*

Pulse Width (μs)	*NDU Before* τ_{Th} *Extraction*	*NDU After single-pole* τ_{Th} *Extraction*	*NDU After Three-pole* τ_{Th} *Extraction*
0.2 μs	0.084	0.085	0.072
2 μs	0.080	0.081	0.065
5 μs	0.079	0.082	0.075
20 μs	0.088	0.091	0.073
50 μs	0.116	0.094	0.075
200 μs	0.175	0.096	0.079
500 μs	0.169	0.089	0.081
1000 μs	0.170	0.076	0.082

From Table.2.2 and Figure 2.11 it can be observed that after single-pole τ_{Th} extraction (by curve fitting) the model seems to predict the device performance more accurately at smaller *W* but fails to predict the measurements at *W* > 20 μs. From Figure 2.15 it can be observed that after the three-pole circuit extraction the new model is able to predict the device performance very accurately from static to very small *W*.

In Table 2.1 Simulation is after the model has been fit to data using Auriga's pulsed I(V) measurements. A graphical representation in linear scale is shown in Figure 2.17.

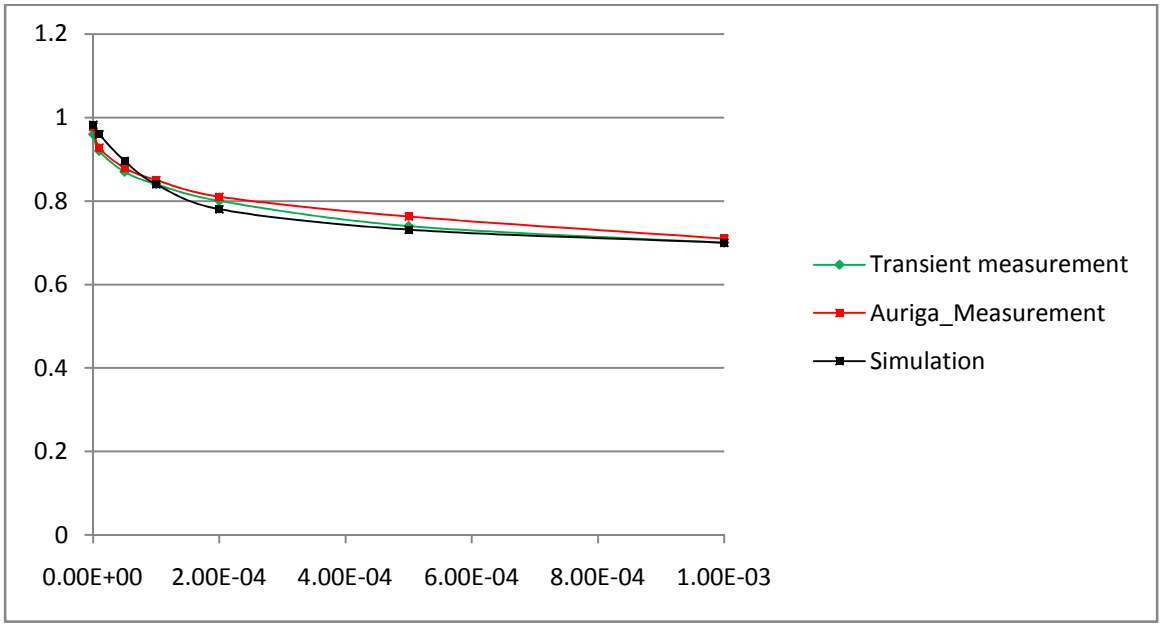
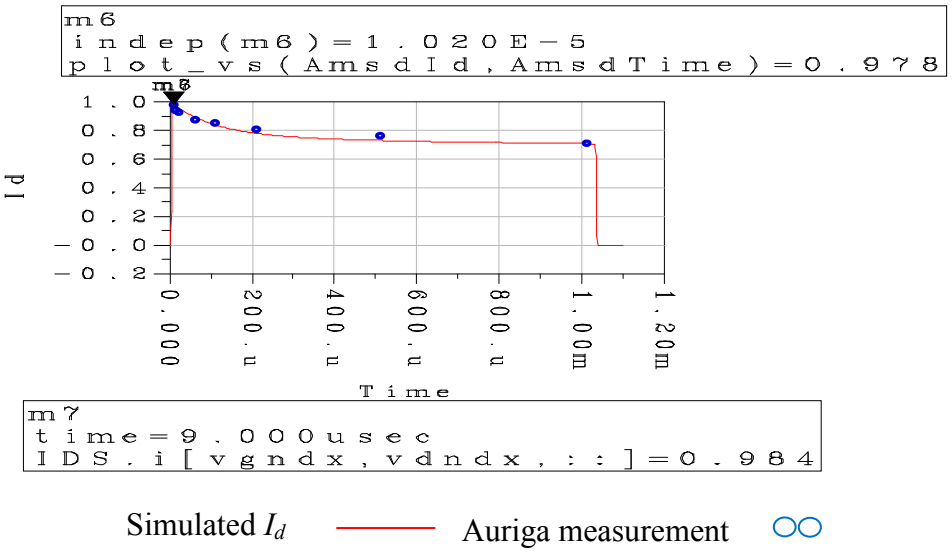
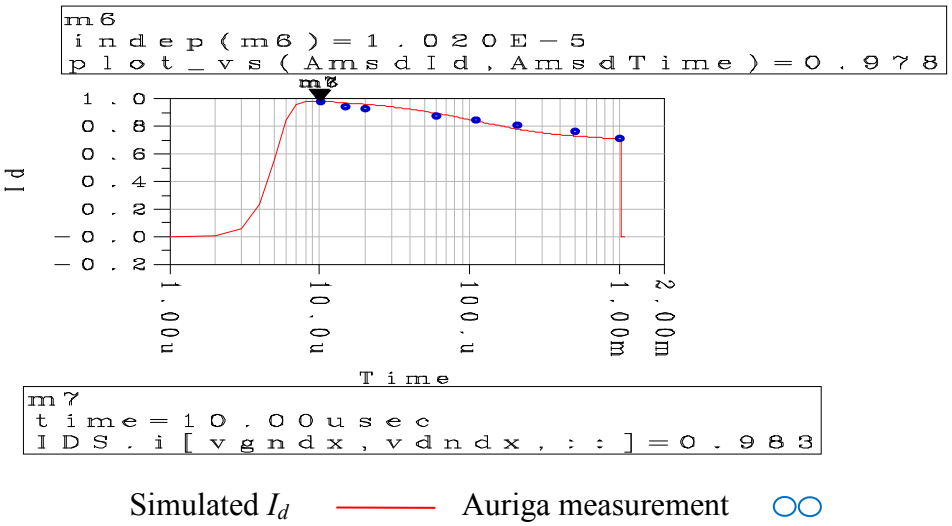


Figure.2.17. Comparison between Transient Measurement, Auriga_Measurement and Modified MET Model Simulation I_d for an LDMOS Transistor

So after careful modification now we have a LDMOS thermal model whose time constant is verified by both the transient method and the Auriga's measurements.



(a) Linear scale



(b) LOG scale

Figure.2.18.Comparison Between the Auriga Measurement and Simulation After Modifying the Thermal Network in Linear and Log Scale

2.7. Summary

In this chapter a new approach was developed for prediction of duty cycle dependent self-heating in LDMOS transistors. A modified MET model has been shown to fit pulsed I(V) measurements for a wide range of duty cycles. The transient current predicted by the modified MET model also agrees very well with a conventional transient measurement.

CHAPTER 3

PULSED LOAD-PULL SYSTEM SET-UP AND CONSIDERATIONS

Pulsed load-pull measurements have several advantages over CW load-pull testing. By using pulsed load-pull we can test an amplifier under the same condition in which it is going to be used, if in fact the final application is pulsed. An example of this kind of application is RADAR or telecommunication base station where the amplifier is used with pulsed or modulated signals respectively. Also pulsed operations may be more linear than CW operation; this is due to the absence of weak thermally induced nonlinearity under pulsed condition [3]. Pulsed operation when combined with high DC voltage levels can also be very interesting for the validation of nonlinear models which take into account thermal and trapping effects, and can be used to test large devices that could not be tested at the same power levels under CW conditions due to excessive self-heating. Pulsed signals can also be used as a first indicator of a power amplifier's peak capability, however complex modulated signals of the final application (IS95, WCDMA.etc.,) should ultimately be used to find the realistic peak power capability of a power transistor under the corresponding thermal loading as shown in Figure.3.1 [19].

New generations of transistors for power applications, in the field of mobile communication systems (e.g. GSM phones and base stations) and radars, require accurate non-linear models applicable for a variety of operating conditions. While non-linear, so-called "compact", models have become widely available for RF transistors, not all

models properly address self-heating effects and in particular the literature shows few treatments that validate the time varying nature of self-heating for slowly varying signals or sufficiently long pulses.

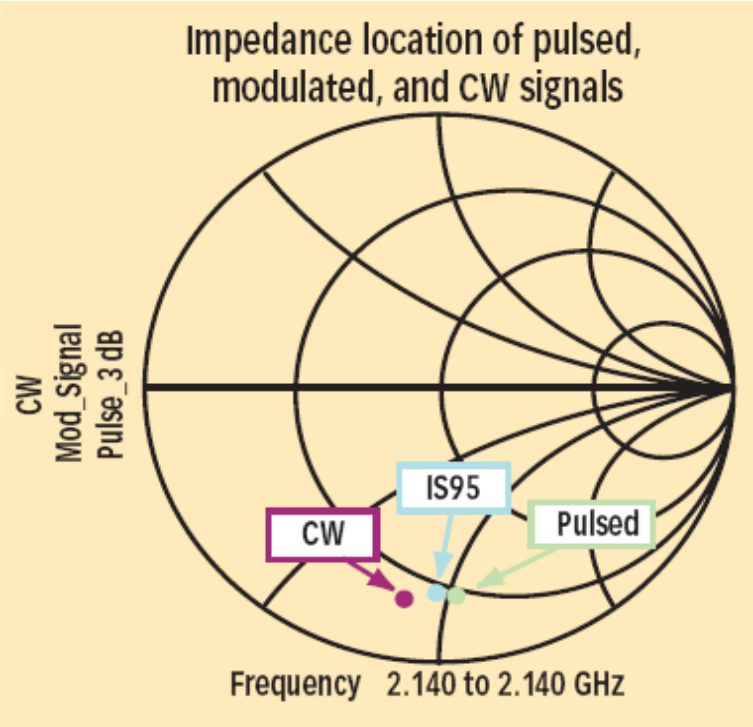


Figure.3.1. Plot showing the optimum load impedance location on the smith chart for CW, IS95 and pulsed modulation formats for a 50 W Enhancement-Mode LDMOS [19]

In particular, some popular technologies (such as VDMOS) that have recently proven their validity in handling high power densities, suffer from thermal degradation of performances, basically due to current collapse. In such cases, electro thermal models are needed to properly predict this degradation. On-wafer measurements of large gate-width power devices can be difficult in CW operation, due to the wafer insufficient heat sinking. To overcome these problems, pulsed operation is becoming more commonly

used for microwave device characterization and model validation measurements [20]. Since then, pulsed I-V and pulsed S-parameter measurements have been widely used to extract electro thermal models of different technology devices [20]-[26]. Such models were generally verified by other (non-linear) measurement techniques, such as load-pull. More recently, the interest in pulsed measurements has grown and the need for pulsed non-linear measurements under different loading and bias conditions has become more clear [27]. One other important requirement to perform pulsed and modulated signal load-pull comes from the fact that these signals exert different thermal loading on the device and consequently the optimum load impedance for each modulation format is also different as shown in Figure.4.1 [19]. The importance of addressing self-heating effects for LDMOS devices has also been pointed out [11], [16] and [28].

Before developing a pulsed load-pull set-up a brief literature review is provided of approaches to pulsed load-pull measurements. A discussion follows of how pulsed RF signals can be generated and how thermal and diode sensors are used for measuring pulsed power and associated dynamic range issues. The limitations and tradeoffs involved with non-ideal switch performance, used to pulse the input is studied to understand that have to be made.

3.1. Background

The literature shows that there are different approaches to construct a pulsed load-pull bench. A pulsed load-pull bench was developed using pulsed bias tees, RF source synchronized using a pulse generator, and digitizing scope in [1] and was used to monitor the current and a peak power meter to monitor the RF power. In this experiment the

pulsed power is achieved by 5µs pulse width on gate side, a 3 µs pulse width for the drain and 2 µs pulse width for the RF signal (f=10 GHZ) [1], the duty cycle was set to 1%. Figure.3.2 shows a comparison between CW and pulsed condition for Pout Vs Pin for the DUT (Device Under Test which was GaN HEMT).

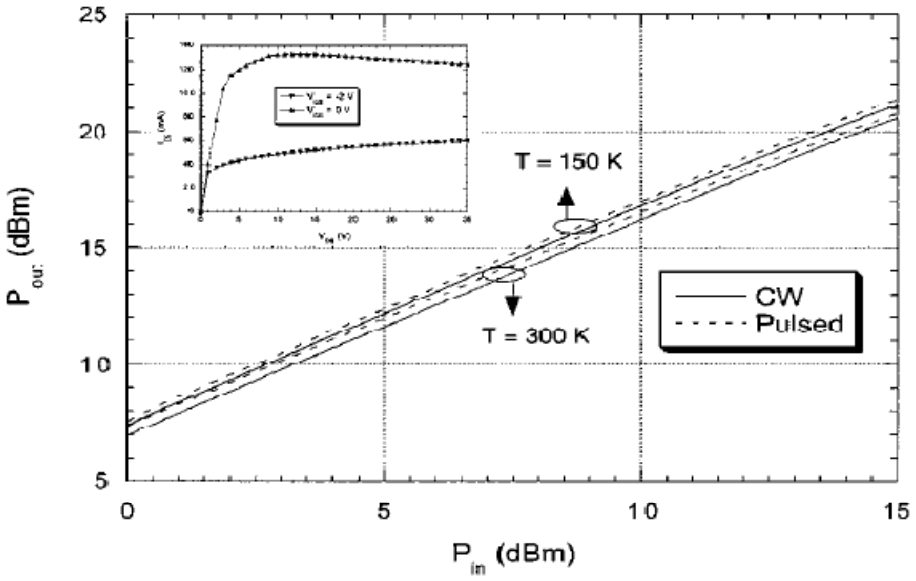


Figure.3.2. P_{out} Vs P_{in} with CW and Pulsed Condition [1]

Pulsed load-pull benches are also constructed using pulsed Vector Network Analyzer (VNAs) and Large Signal Network Analyzer (LSNAs). For example, a pulsed load-pull test bed was developed for characterizing high voltage HBTs using a pulsed VNA to monitor the RF power profiles and sampling scope to measure the DC current/profiles [2]. In this paper a pulse modulator connected to the output of the microwave source is used to create the stimulus signal while four other pulsed modulators are used to scan the pulse duration from the beginning to the end of the pulse stimulus to see the response of the Device Under Test (AlGaN/GaN Power HEMTs), in this case a high voltage HBT. Figure.3.3 shows the block diagram of the set-up

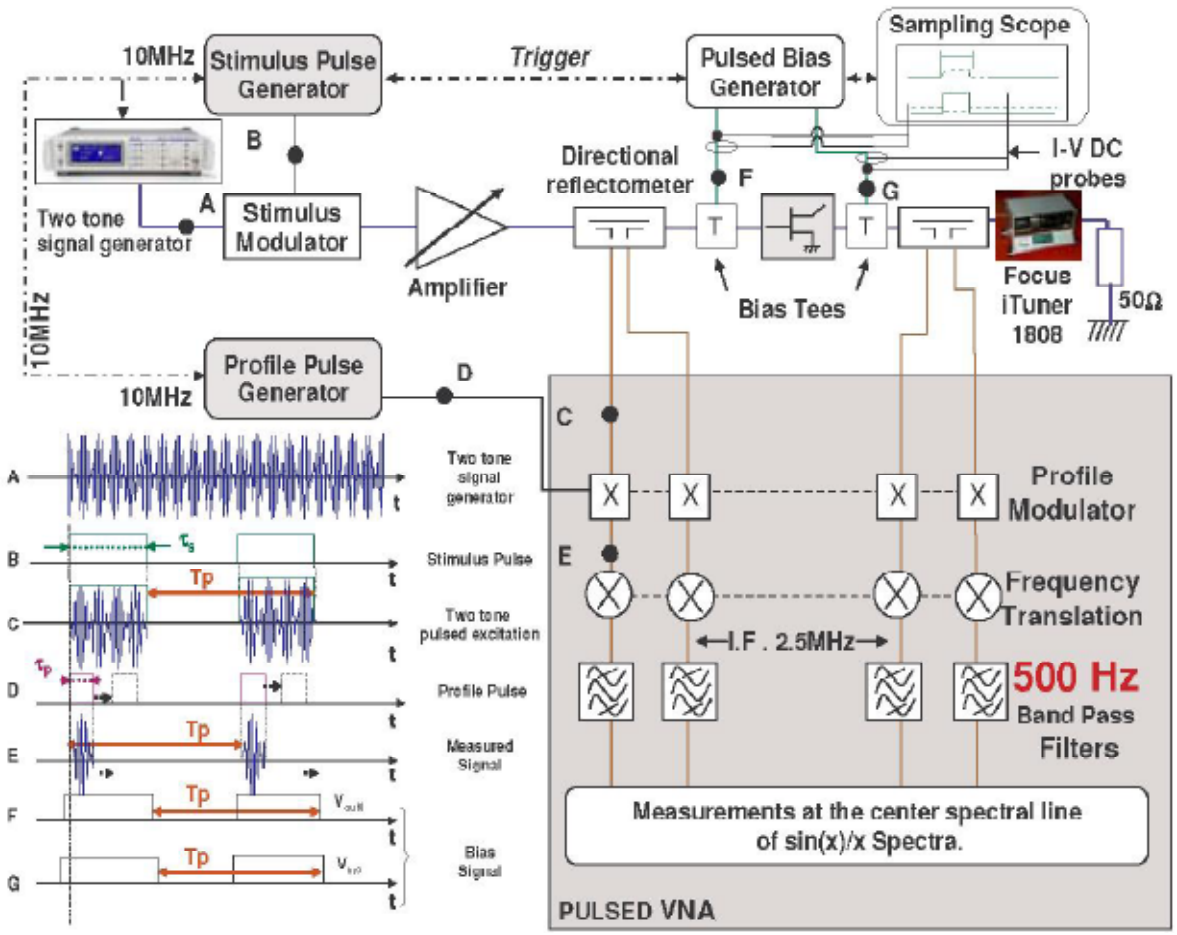


Figure.3.3. Block Diagram of the Pulsed Load-pull Set-up [2]

From the above diagram it can be observed that the stimulus modulator is used to pulse the CW signal and the other pulse modulators are used to set the profile of the pulse so that the response of the DUT at a specific time inside the stimulus can be observed. Pulsed bias generator and sampling scope are used to pulse and measure the DC bias. The pulse profiling (measurement time window) is given in Figure.3.4.

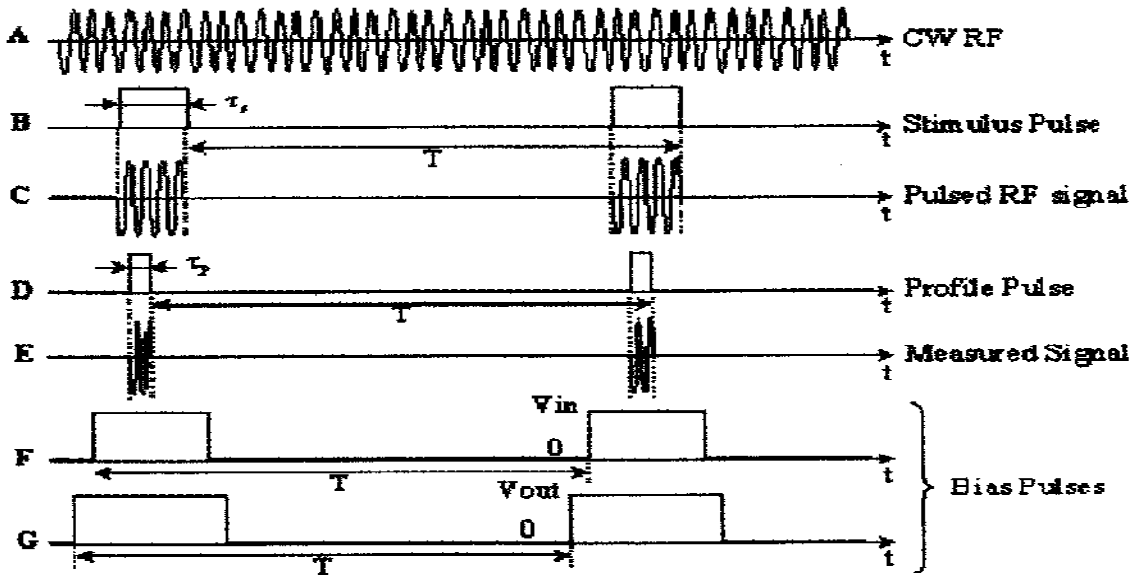


Figure.3.4. Pulsed RF and Bias Signal Representation [2]

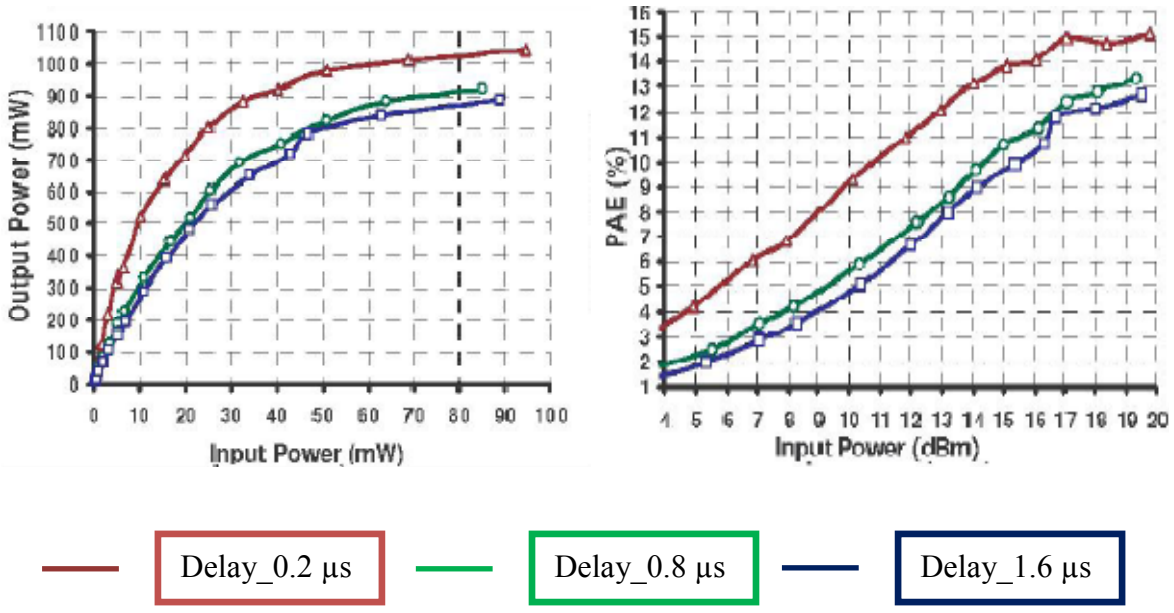


Figure.3.5. (a) Pout (mW) Vs Pi (mW) and (b) PAE Vs Pin (mW) of High Voltage HBT [2]

The authors of this work have demonstrated that using a pulsed VNA as part of a pulsed load-pull allows control and synchronism of the repetition rate and the RF pulse

width as well as the profile acquisition window. From Figure.3.5 it can be observed that we have more Pout and PAE at the beginning of the pulse and decreases as the duration within the pulse increases which clearly shows heating effect of the transistor.

3.2. Power Sensor Operation

Thermal or average sensors estimate peak pulse power using a theoretical correction based on knowledge of the duty cycle. This is done by use of average-power responding sensor and dividing the result by the pulse duty cycle to estimate the peak power. This is suitable only if the modulation waveform is a rectangular pulse with a known and constant period. Recent peak-power meter designs have started to use advanced signal-processing to detect and analyze the actual modulation envelope of the signal, and to use time-gated systems that measure the power only during the ON portion of a pulse [29].

Diodes convert high-frequency energy to DC by means of their rectification properties, which arise from their non-linear current-voltage characteristics. Figure.3.6 shows a typical diode detection curve starting near the noise level of –70 dBm and extending up to +20 dBm. In the lower "square-law" region the diode's detected output voltage is linearly proportional to the input power (Vout proportional to Vin) and so measures power directly. Above –20 dBm, the diode's transfer characteristic transitions toward a linear detection function and the square-law relationship is no longer valid [29]. Modern power meters perform a non-linear correction to extent the usable dynamic range of diode sensors as discuss next.

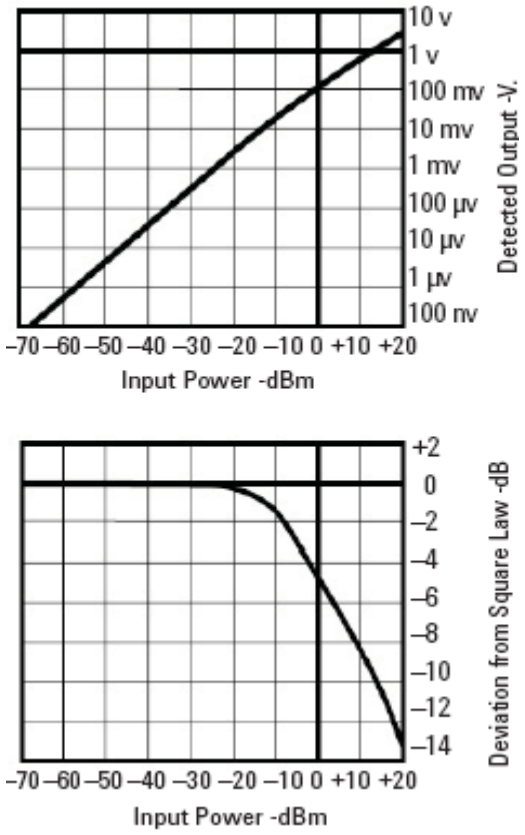


Figure.3.6. Diode Detection Characteristic Range from Square Law Region Through the Transition and Linear Region [29].

To make the diode sensor read accurate power beyond the square law region we need an ideal sensor that would combine the accuracy and linearity of a thermal sensor with the wide dynamic range of the corrected diode approach [29]. One other important factor of a diode sensor is the video bandwidth, video bandwidth is the bandwidth detectable by the sensor and meter over which the power is measured, and is sometimes referred to as the modulation bandwidth. It is generally recommended that the power sensor should have a rise time of no more than *1/8* of the expected signal's raise time [30]. For example the rise time of the pulse signal used at USF is 45 ns (from the UMTS

switch datasheet) so we need a sensor with a raise-time of < 5.6 ns in order to measure accurate pulsed power.

3.3. Pulsed Power Theory

Before taking a look at the comparison of the sensors, some basic terms related to pulsed power should be reviewed; for example the duty cycle of a pulsed signal is given in terms of the pulse width τ and the period T as [31]

$$Duty\ Cycle = \frac{\tau}{T} \tag{3.1}$$

Thus the duty cycle of the RF pulse can be increased by either increasing the pulse width or decreasing the time period of the RF signal. The Pulse Repetition Rate (f_p) is the frequency at which the pulses occur and is given by

$$f_p = \frac{1}{T} \tag{3.2}$$

The use of a thermal sensor was examined first. A thermal sensor calculates the pulsed power P_p in terms of average power P_a as follows [32]:

$$P_p = \frac{Pa}{\tau\, fp} \tag{3.3}$$

where f_p can be calculated by (2), τ is the pulse length and P_a is the average power. It is important to keep in mind that the above relationship holds good only if the pulses can be assumed to be rectangular in shape. When the pulse shape is irregular it may lead to erroneous power measurements and so a shape factor correction must be applied, which may be subject to a relatively large uncertainty [32].

In the second set of measurements, a diode sensor was used. Diode sensors are capable of measuring pulsed power due to their fast raise time. Diode sensors can be used to predict the peak voltage of the RF signal. The relation between the peak RF voltage and the rms power P_{rms} is given by [33] as

$$P_{rms} = \frac{(Vp \times 0.707)^2}{R} = \frac{Vp^2}{2R} \qquad (3.4)$$

where R is the resistance of the load across which the diode is connected.

To validate or qualify a pulsed power system all the factors that influence it have to be taken into account. In an attempt to isolate the effects of duty cycle on the pulsed measurement results, multiple measurements of pulsed power were taken in which the time period was kept constant and the duty cycle was changed by varying the pulse width. When the pulsed power is derived from an average power measurement (as in the case of the thermal sensor), the dynamic range is reduced as the duty cycle is lowered. The reduction in dynamic range from a CW measurement for a pulsed power measurement with period T and pulse length τ can be estimated by

$$\text{Reduction in Dynamic Range} = 10 \log \frac{T}{\tau} \qquad (3.5)$$

3.4. Measurement Set-up Used to Explore Switch and Sensor Performance

A symbolic representation of signals at different ports of the RF switch is depicted in Figure.3.7. Port A is the input port, port B is the signal applied to the control port of the switch, and port C is the output of the switch that is input to the device under test. Figure3.8 shows the measurement set-up, which includes a thermal sensor (Anritsu

MA2422B or a diode sensor (Anritsu MA2411B) an RF switch (e.g. UMCC - model # SR-T800-2S RF switch, or a Mini-Circuits _XXYY switch), a power meter (Anritsu ML2496A pulsed power meter or Anritsu ML2438A power meter), a signal generator (e.g. HP 8648C), and a digital delay generator (Highland P400). The Automated Tuner System (ATS) measurement software from Maury Microwave [34] was used to automate the measurements and make system loss corrections as applicable. The delay generator was used to provide the necessary logic control for the RF switch. An active-low switch was used for the measurement: when the digital control pulse is low, the switch passes the RF input through the switch.

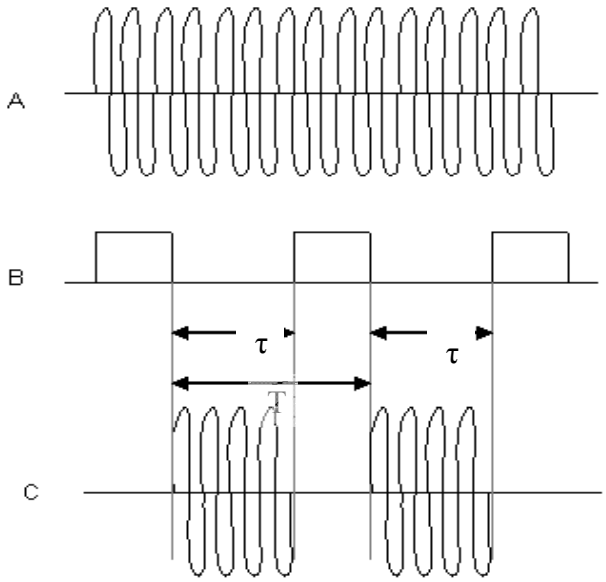


Figure.3.7. RF Signal Representation at Ports A, B, and C of the RF Switch as shown in Figure.3.8

The pulsed power calibration for a specific pulse set-up, is performed by changing the pulse width τ of the control logic of the delay generator so that the pulse B shown in

Figure.3.7 corresponds t › the desired characteristic. The RF switch TTL low allows the RF signal at to pass thro ıgh it. The calibration of the system showed tha: the system had an input insertion loss, b ɛfore the DUT, of -2.451 dB. The ATS software corrects for such losses as a result of the calibration procedure. The reduction in dy amic range as pulse length is decreased for a thermal sensor can be seen when a calibr tion is performed. The basic set-up of Figure 3.8 was used to perform various experiments whose goal was better u derstanding of potential limits introduced by th ɛ non-ideal nature of the RF switch s well as the power sensors for varied duty cycle swept power testing. These results ar › shown in Chapter 4.

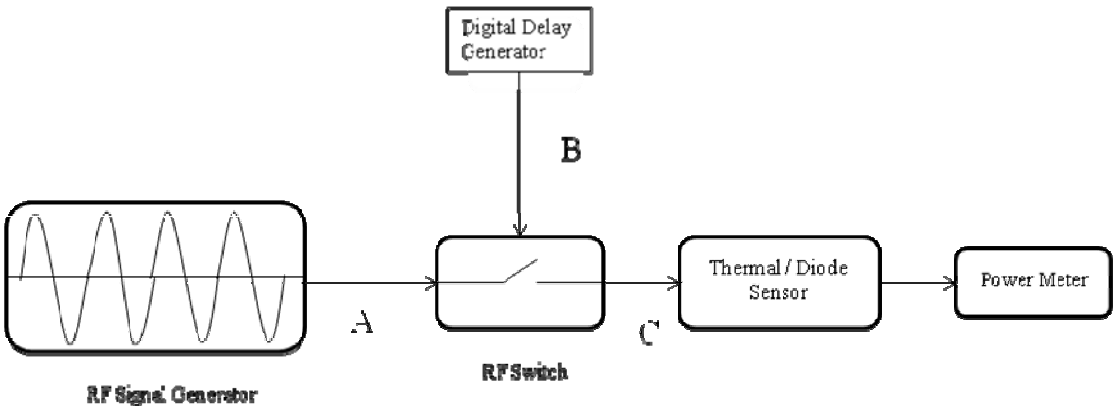


Figure.3.8. Pulse Powe · Measurement Set-Up Used for Switch and ·ower Sensor Experimentation

3.5. Pulsed Load-pull Theory

To understand pulsed load-pull a clear understanding of basic load-pull measurement is essential. Load-pull in the simplest form consists of a DUT with a calibrated tuning device on its output. The input will also be tunable but this is mainly to boost the power gain of the device and will be changed according to each frequency to get a good input match. Load-pull is used to measure some important parameters like power compression, gain, inter modulation distortion (IMD) measurements, saturated power, efficiency and linearity as the output is varied across the smith chart. Load pull analysis is used because a network analyzer can only measure the *small- signal* response of an active device but it is not possible to measure the performance under *large- signal* conditions. In small-signal operation the variation around the transistor quiescent bias point is small enough that the behavior of the signal characteristics appears linear, whereas in large-signal model the variation about the quiescent bias point is larger and the small-signal model is no more valid. This is where the load pull becomes important because it can be used to gather data needed to predict the large-signal performance of the active device.

Analyze of the load pull data is done by using a Smith chart and plotting contours of constant output power, gain, and efficiency as shown in Figure.3.9 One observation that can be made by looking at this figure is that unlike noise circles the power contours are often not circular unlike noise circles no matter how carefully the system is calibrated.

The explanation for the shape of the load-pull power contours has been given in [35]. The first step in any load pull system is accurate S-parameter measurement of all the

blocks in the system. To obtain this the VNA should be calibrated very carefully. Doing this will remove the effect of tuners, cables, connectors, attenuators, probes, and all other components in the system and shift the reference plane for measurement to the probe tip or the DUT. Once the VNA is calibrated and S-parameters of the individual blocks are measured, utmost care should be taken that the set up is not disturbed. Figure.3.10 shows the different blocks involved in a load pull set-up.

For this work a Maury Microwave Load-Pull test system was utilized along with the Maury "ATS" Software, which is used for system calibration and measurement. Calibration includes careful VNA measurements of all of the system components in the RF path between the signal generator and the power sensor and/or spectrum analyzer used to perform power or spectral measurements for varied source and load impedances.

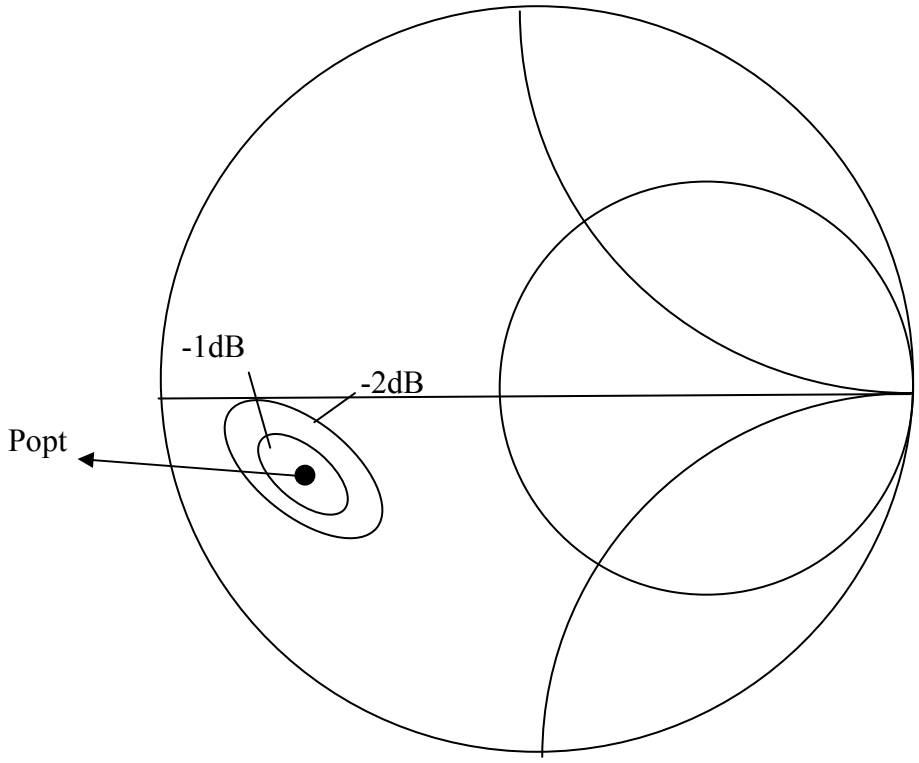


Figure.3.9. Typical Load-pull Data [35]

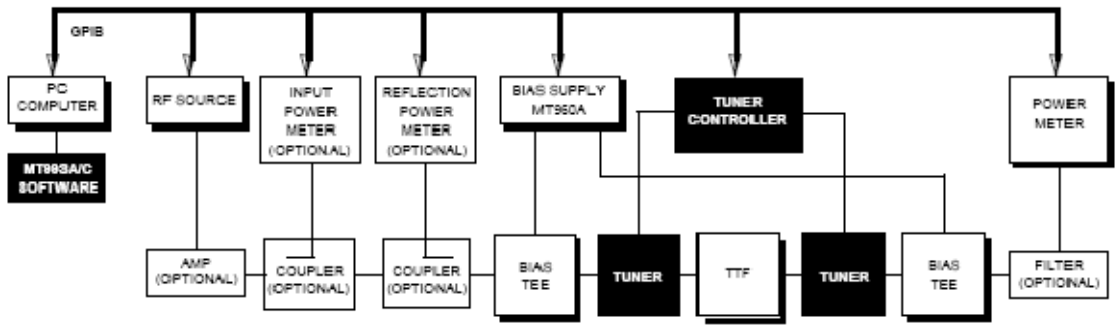


Figure.3.10. A Representative Load Pull Set Up [34]

After calibrating and saving the S-parameter files for all components they are entered into the ATS Maury Software and the software controls the instruments and tuners. Figure.3.11 shows the various blocks for which the S-parameter has to be measured and stored. Tuner characterization consists of performing VNA testing of the source and load tuner blocks for many different impedance settings of the tuners for each frequency the load-pull testing is to be performed.

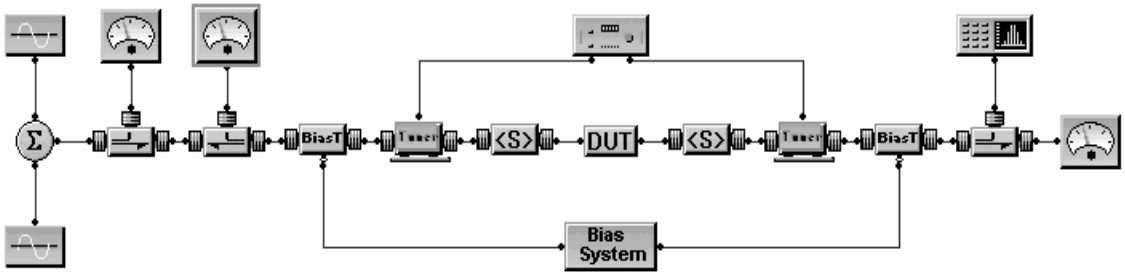


Figure3.11. Different Blocks Involved in a Typical Power/Intermod Measurement [34]

3.6. Calibration Checks

Before measurement the characterized tuners data is entered into memory for both the tuners. This includes the measured 2- port complete S-parameter data and the corresponding tuner position for a number of discrete tuner positions. The tuner is considered as the heart of the load pull set-up so it has to be characterized properly to get accurate measurements. Before characterizing the tuner, the VNA should be calibrated using proper high reliability cables and connectors. Set the start, stop and step size for the frequency and then in cal type select Full 12 – term. Enter the values for the terms from the calibration data sheet available. To check the VNA calibration performed connect the thru and capture the data and plot S12 and S21 +/- 0.1 dB and the reflection coefficients |S11| and |S22| should be < -40 dB. Then connect open on both ports and |S11| and |S22| should be < + or – 0.05 db, then connect short and |S11| and |S22| should be again < + or - 0.05 dB. Similarly after the tuner is characterized perform the same set of tests that was explained in the previous steps to ensure your calibration.

Extra care should be taken after calibrating the VNA so that the cables do not bend and minimum movement should be allowed. Now connect the tuner to the VNA. The tuner's position will be changed automatically by the tuner controller and the S-parameter for different tuner positions will be saved in the system. After doing all the calibrations and obtaining the tuner datas, the set-up can be verified using this procedure: based upon the small-signal S-parameters that were entered for each block the software will calculate a transducer gain Gt(s). The software measures the actual transducer gain Gt which is the delivered output power to the available input power at the DUT reference plane. ΔGt is the difference between Gt and Gt(s); it should be less than 1or 2 db. After

these steps, power or intermodulation calibration has to be done before taking the actual measurements. In pulsed load pull, the input RF single tone is pulse modulated by a pulsed RF source or an RF switch whose pulse width can be altered as desired.

3.7. Pulsed Load-pull Set-Up:

The pulsed load-pull system used in this work is shown in Figure 3.12 with changing duty cycle from CW to short pulse. The system uses an HP signal generator followed by an RF switch driven with a pulsed source, an Anritsu thermal sensor and power meter in combination with a Maury Microwave load pull system. The whole system was controlled using Maury Automated Tuner System (ATS) software. The advantages of pulsed load-pull and CW load-pull were clearly seen in the results of the experiment. It was observed that pulsed load-pull allowed the device to be safely driven to higher pulsed powers as the duty cycle was decreased.

In this set-up the UMCC - model # SR-T800-2S RF switch (1-18 GHz) was used to pulse the input before the preamp, the power meter used was an Anritsus ML2438A along with Anritsu thermal sensor MA2422B. A 10 W enhancement-mode vertical MOSFET was used for this experiment.

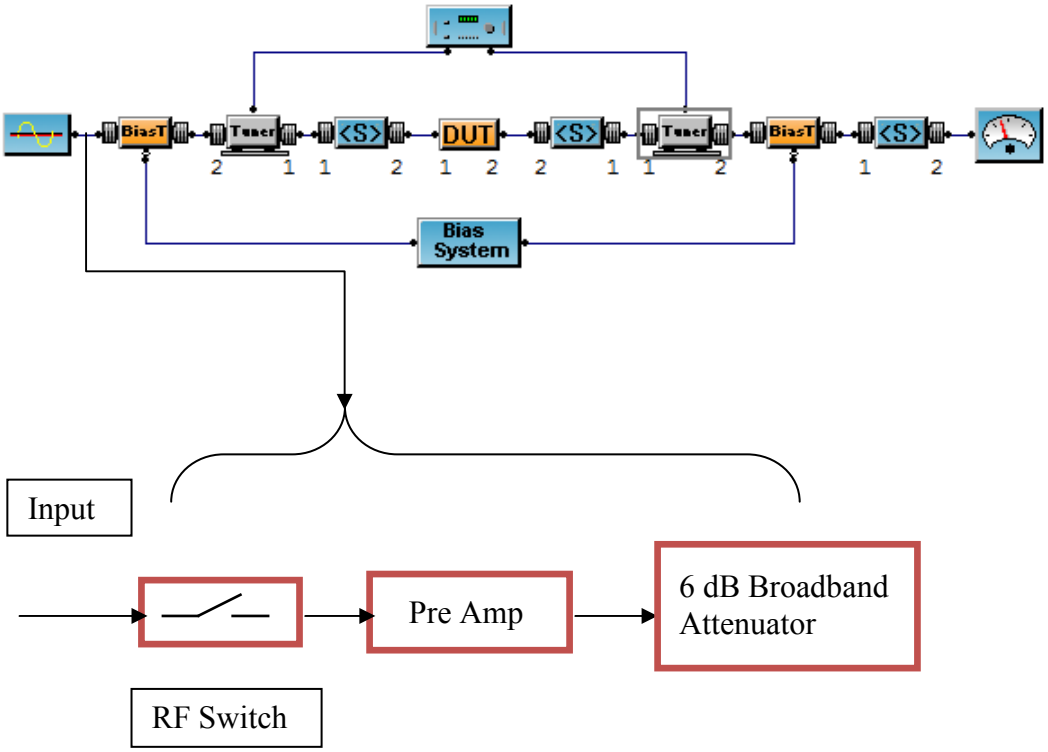


Figure.3.12. Pulsed Load-pull Set-up

There were some problems with this set-up

1) When the input RF signal was pulsed with time period 2ms and pulse width 200µs (Duty Cycle = 10%) the dynamic range issue and noise floor began to increase for the thermal sensor.

2) The formula used by Maury to calculate efficiency is given by

$$\text{Efficiency} = 100 * \left(\frac{Pout - Pin}{Vout * Iout + Vin * Iin}\right) \qquad (3.6)$$

The problem with this is when the input RF signal is pulsed the drain current I_d from the device is also in a pulse shape and since the DC signal is not pulsed a manual correction may be needed to obtain the desired value of efficiency which is explained later.

3) Another issue is when the duty cycle is decreased by reducing the pulse width or increasing the time period the dynamic range of the thermal sensor starts to reduce as the noise floor creeps up. So for small duty cycle it is advisable to use the pulsed diode sensor.

3.8. Summary

In this chapter we reviewed various set-ups that have been used by others for pulsed load-pull testing. A custom test bench used in this research was then described. This bench was used with some variations for both benchmark testing of switches and power sensors as well as the pulsed load-pull experiments described in the next chapter. The differences between use of pulsed and thermal power sensors and related dynamic range trade-offs were explored experimentally.

CHAPTER 4

PULSED LOAD-PULL SYSTEM EXPERIMENTATION AND MEASURED RESULTS FOR SELECTED RF POWER TRANSISTORS

In this chapter results are presented first for various system experiments conducted to better understand limitations of various components like the input RF switch, the power sensor [36] and the bias tee (See Appendix A). Following this, pulsed load-pull results are shown for two example high power RF power transistors: one a VDMOS device and the other an LDMOS device.

4.1. Results of Switch and Power Sensor Experimentation

In Figure.4.1 power testing results are shown for the case of a thermal sensor and a switch manufactured by UMCC SR-T800-2S. Figure.4.1 shows the measured pulsed available power (at the sensor) versus the programmed power for various pulse lengths and a constant period of 100 μs and RF signal frequency 2GHz. As we will point out, the best approach to calibration and use of a thermal sensor is to calibrate under CW conditions, then use the pulsed input stimulus for the DUT testing only (not calibration). The Y axis ($P_{available}$) is the pulsed power calculated by Maury automatically when f_p and τ are known. It is important to note while observing this data that the thermal sensor measures average power. For reduced pulse length (and hence reduced duty cycle) a reduction in the dynamic range of the sensor was observed due to the fact that the power

is applied for a shorter amount of time, thus decreasing the average power delivered to the sensor. The thermal sensor used has a manufacturer specified dynamic range of -30dBm to 20dBm. Figure.4.1 shows that as expected the sensor actually has an absolute low end that is lower than its specification (to provide some margin). For a 50 % duty cycle (in the Figure.4.1 case a 50 μs pulse length), the average power detected by the sensor at each pulsed power setting is approximately 3 dBm lower than in the continuous-power case. For the 50 % case, it would be expected that a pulsed power of -30+3 = -27 dBm would be the lowest pulsed power recommended to be measurable by the sensor, based on the specified range.

For a duty cycle of 5 percent (5 μs pulse length) the average power that can be measured in each setting is reduced by approximately 13 dB, this effect can be clearly observed from Figure.4.1. In Figure.4.2 the same plot with Y axis as average Pout (available) is shown. Here it can be clearly observed that the lower limit of the sensor is actually around -39 dBm where it hits the noise floor. Because the specification for the low-power measurement limit of the sensor is -30 dBm (the actual observed lower limit during the experiments was -34 dBm), for the case of a 5 percent duty cycle, the lower limit for pulse power is (-30 + 13) = -17 dBm. This is consistent with the results in Figure3.4. (a). The results in Figure.4.1 (b) indicate that this setting allows measurements to about -20 or -21 dBm (the sensor seems to show a trend of possessing a “noise floor” about 3 or 4 dB lower than would be calculated from the specification).

Due to the noise and reduction in dynamic range as the duty cycle is reduced, deterioration in the precision of the measurements can be observed. From Figure.4.1 it can be seen that the low pulsed-power measurement limit of the sensor is relatively high

for very low pulse lengths. In Figure.4.2 it can be seen that for 0.5 µs the sensor response is in the noise floor until a Pin of -11 dBm. At 0.1 µs the lowest power ($P_{available}$) that could be accurately measured is -4 dBm. This low duty cycle deterioration is present for both calibration as well as DUT testing.

Further experimentation was performed using calibration under both pulsed and CW conditions, and these tests showed that the best approach is to calibrate under CW conditions prior to performing DUT testing under the desired duty cycle. The reasoning for this is sound: the sensor measures average power, so calibrating with larger average power values will enhance the precision of both the calibration and the ensuing measurements.

Figure 4.3 shows the calibration results using a diode sensor (for comparison with Figure.4.1). It can be observed that the diode sensor exhibits no low-power dynamic range issue for pulses tested between 90 and 0.5 µs. For pulse lengths below 0.5 µs, some problems are observed with the diode sensor measurements.

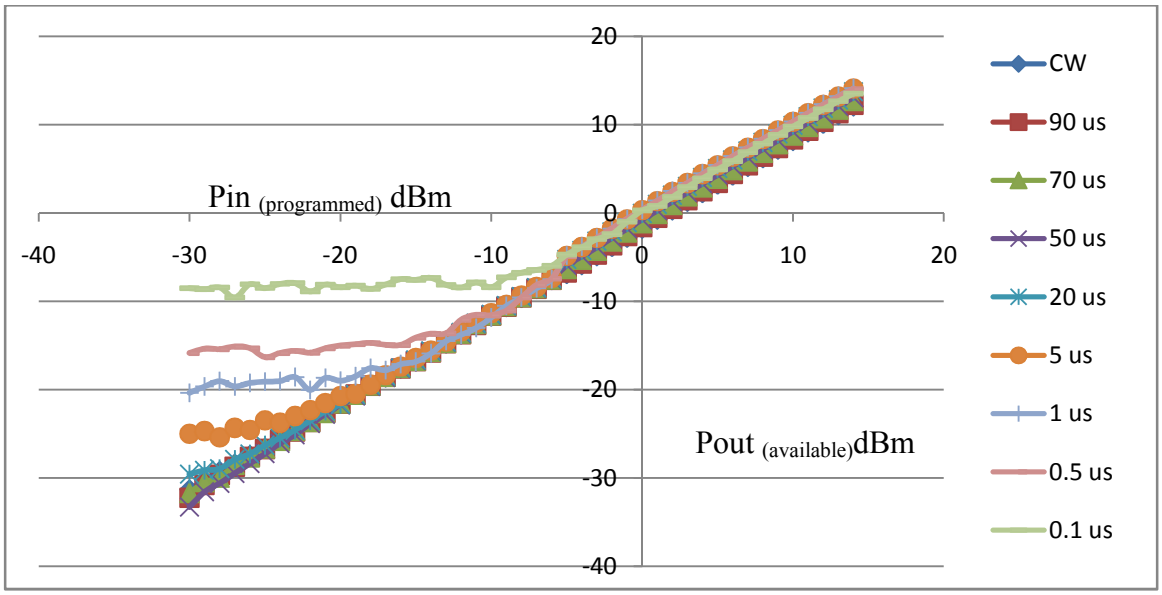


Figure.4.1. Calibration Data: $Pin_{programmed}$ Versus pulsed $Pout_{available}$ for Thermal Sensor for Various RF Pulse Width and Constant Period of 100 µs

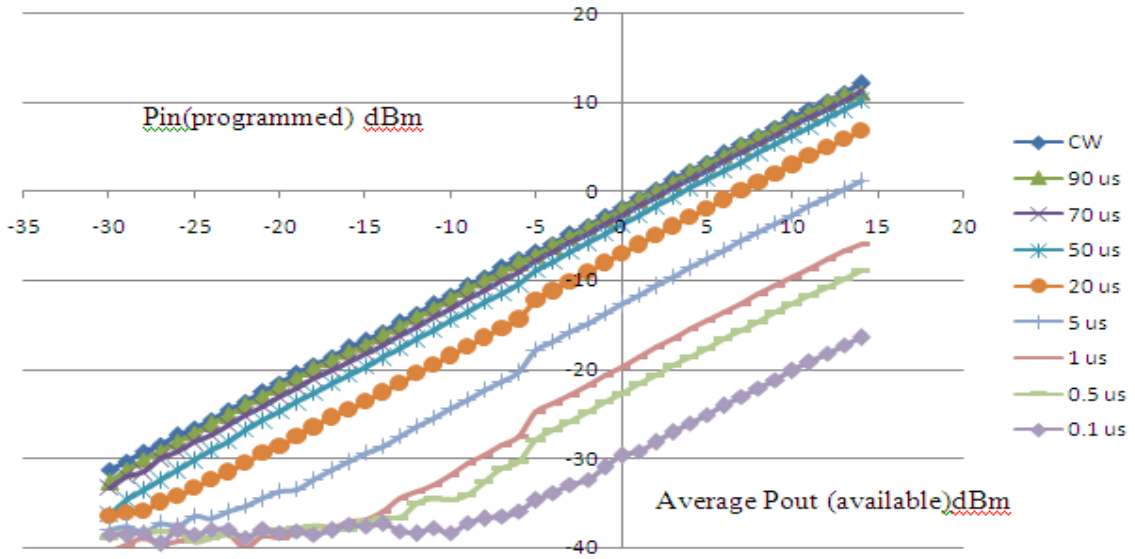


Figure.4.2. Calibration Data: $Pin_{programmed}$ Versus Average $Pout_{available}$ for Thermal Sensor for Various RF Pulse Width and Constant Period of 100 µs

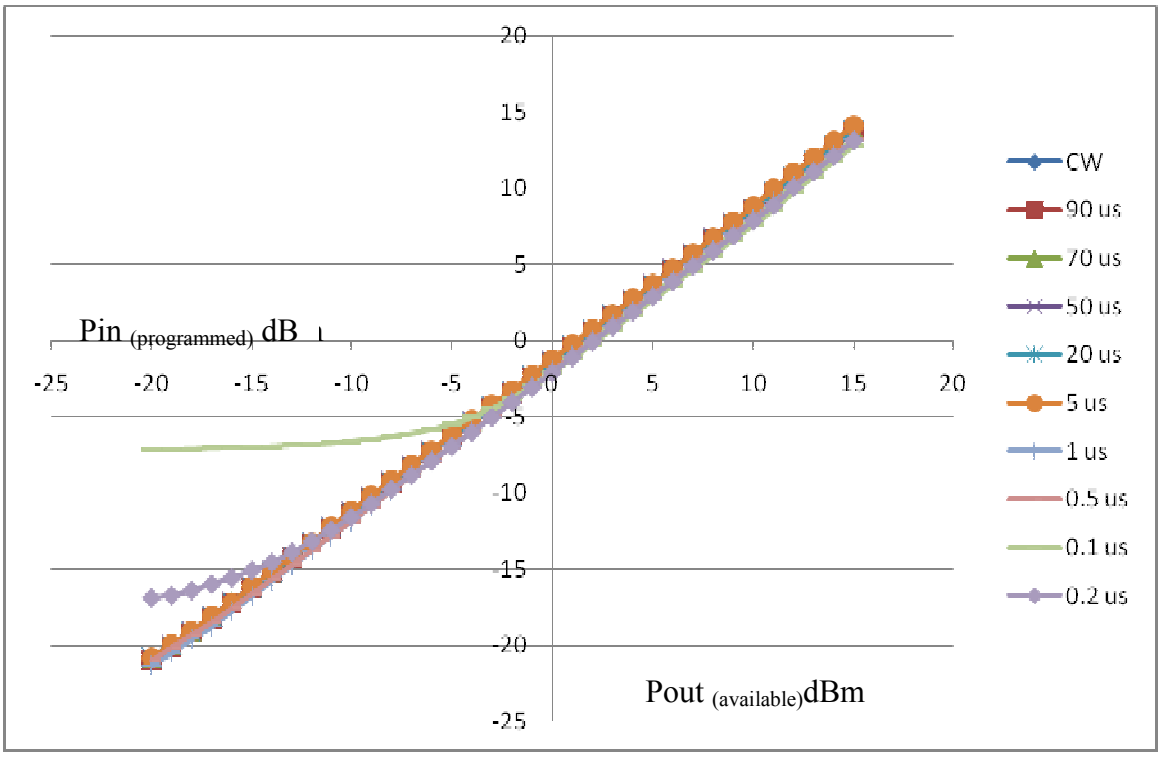
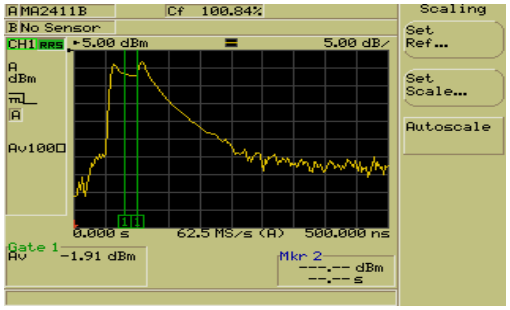
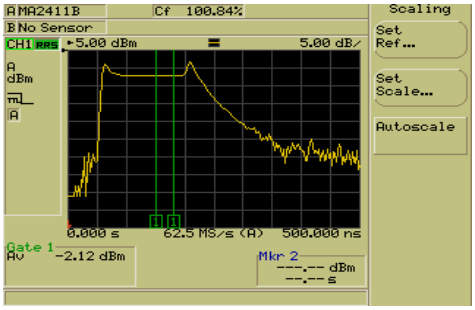


Figure.4.3. Calibration Data: $P_{available}$ Versus $P_{programmed}$ for Diode Sensor for Various RF Pulse Width and Constant Period of 100 µs with UMCC Switch

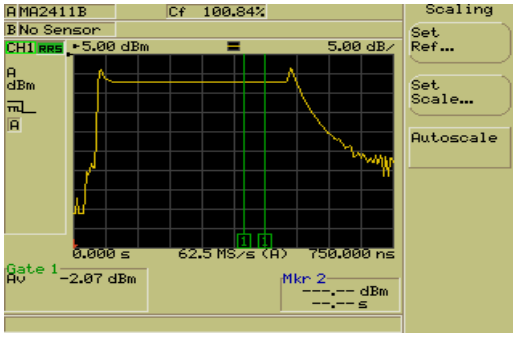
Since a diode sensor uses gate to measure the peak voltage and calculates pulsed power as shown in equation 3.4 it is more accurate, so we did a thorough analysis of the set-up and found that the switch was limiting the smaller pulse widths. Figure.4.4. shows power versus time as viewed by the power meter for several different pulse lengths at an input power of 0 dBm. The power meter has been configured to report the average power measured between the two vertical cursors shown on the screen view. Figure.4.5 shows the power-versus-time view for a significantly lower input power value (-20 dBm).



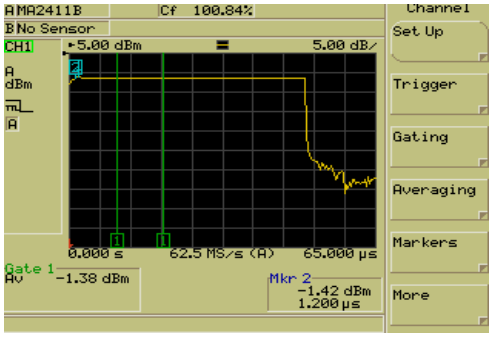
(a) Pulse Width = 0.1 µs



(b) Pulse Width = 0.2 µs

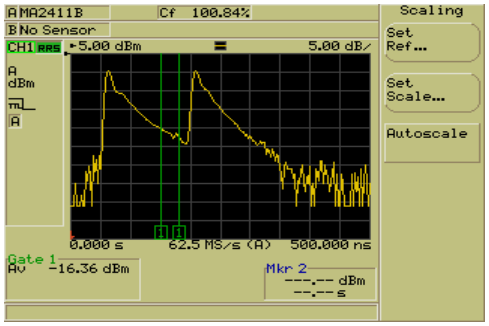


(c) Pulse Width = 0.5 µs

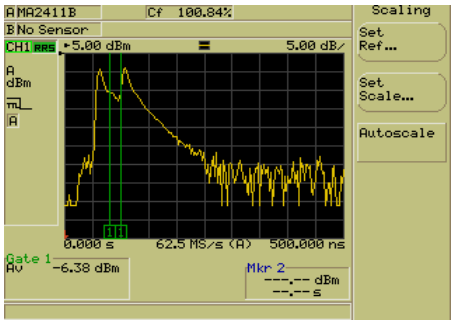


(d) Pulse Width = 50 µs

Figure.4.4. Power Meter Screenshots of Power Versus Time for Different Pulse Widths for T = 100 µs and $P_{Programmed}$ = 0 dBm with UMCC Switch



(a) Pulse Width = 0.1 µs

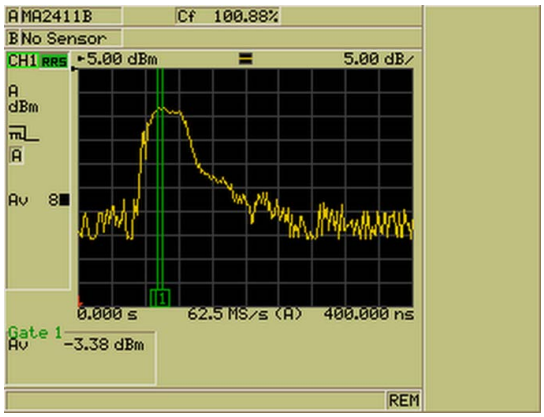


(b) Pulse Width = 0.2 µs

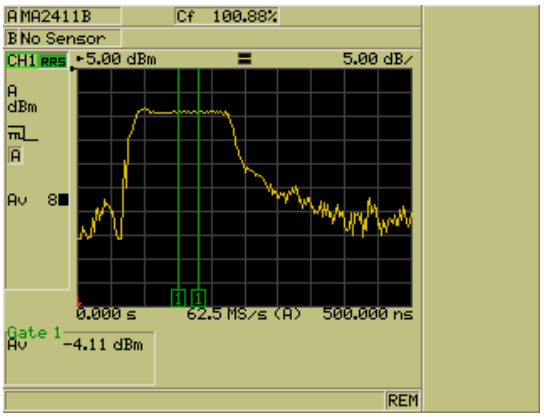
Figure.4.5. Power Meter Screenshots of Power Versus Time for Different Pulse Widths for T = 100 µs and $P_{programmed}$ = -20 dBm with UMCC Switch

In this case, it appears that, while a satisfactorily flat region can still be used to obtain a reasonable measurement at the 0.5 µs pulse length, the power trace in the 0.2 and 0.1 µs cases appears very uneven, and it is difficult to place the cursors to get an accurate measurement. This seems to be a reasonable explanation for the difficulty in obtaining accurate low-power calibrations for the 0.1 and 0.2 µs pulse lengths in Figure.4.3. It was concluded that caution should be exercised when attempting to measure using this set-up for 0.1 µs and 0.2 µs pulse lengths for low power values.

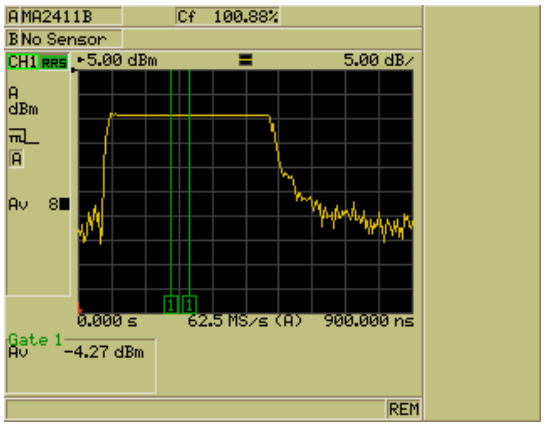
The use of a different RF switch (Minicircuit ZFSWA-2-46) has been shown to produce more favorable results for these lower duty cycles as shown in Figure.4.6 and Figure.4.7.



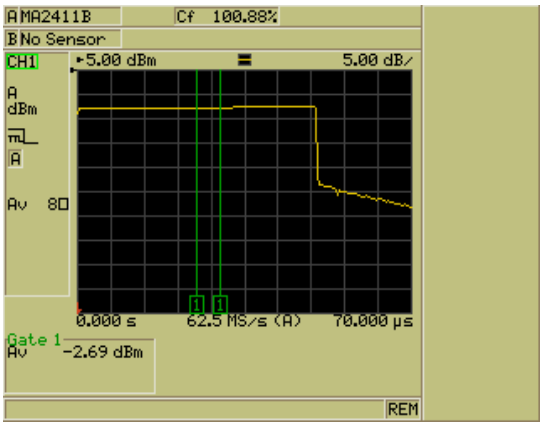
(a) Pulse Width = 0.1 µs



(b) Pulse Width = 0.2 µs

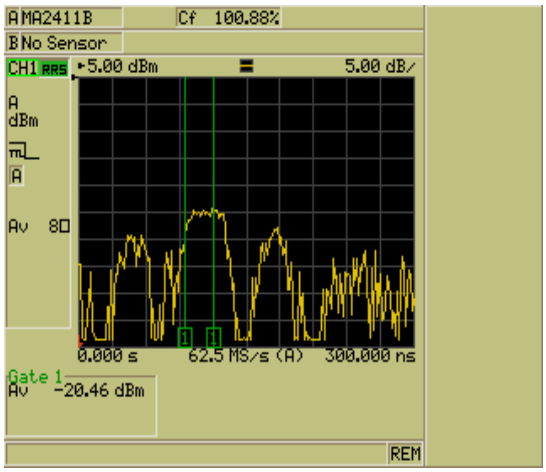


(c) Pulse Width = 0.5 µs

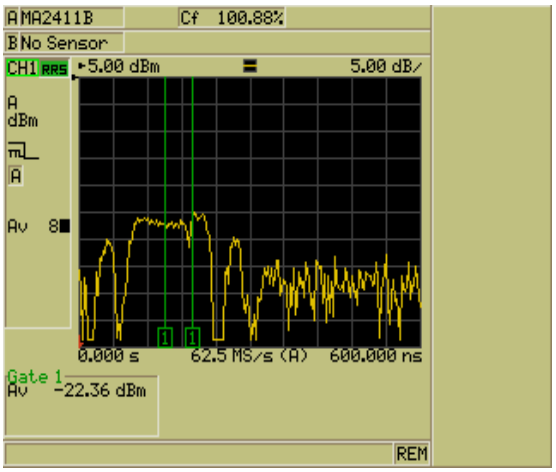


(d) Pulse Width = 50 µs

Figure.4.6. Power Meter Screenshots of Power Versus Time for Different Pulse Widths for T = 100 µs and $P_{Programmed}$ = 0 dBm with Minicircuits Switch



(a) Pulse Width = 0.1 µs



(b) Pulse Width = 0.2 µs

Figure.4.7. Power Meter Screenshots of Power Versus Time for Different Pulse Widths for T = 100 µs and $P_{programmed}$ = -20 dBm with Minicircuits Switch

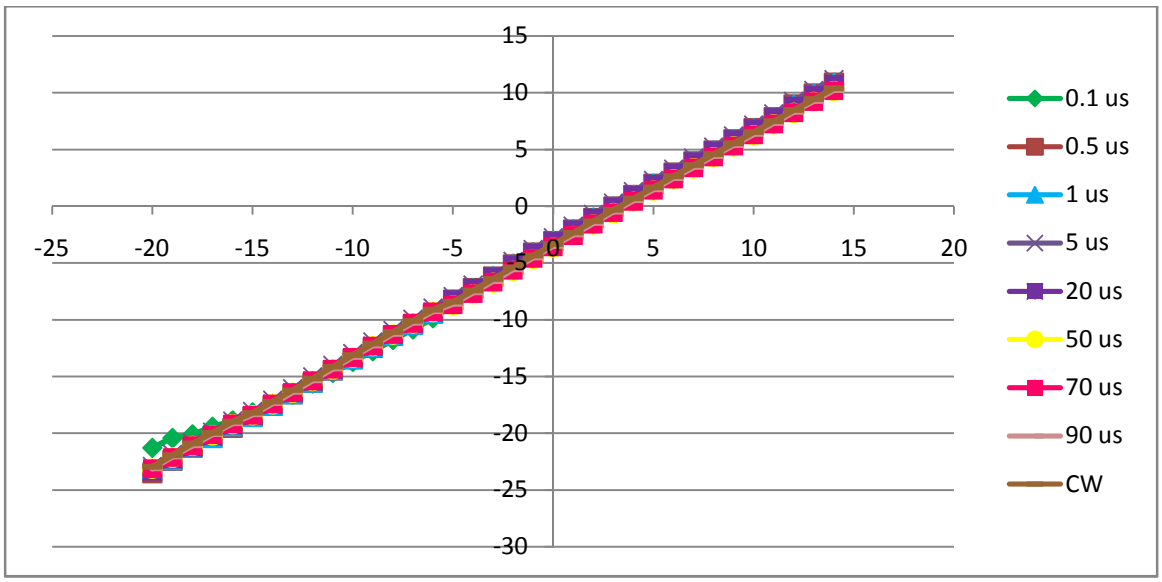


Figure.4.8. Calibration Data: $P_{available}$ Versus $P_{programmed}$ for Diode Sensor for Various RF Pulse Width and Constant Period of 100 µs with Minicircuits Switch

From Figure.4.8 it concluded that the Minicircuit Switch has a much better response for lower pulse widths. Figure.4.9 shows a comparison between the measured Gt of the thru for both of the sensors at a pulse length $\tau = 0.5$ μs pulse length during a power sweep. For these results the set-up with the UMC switch was used. Ideally Gt should be zero for all power levels, but it can be observed that the thermal sensor loses precision at lower input power values. Also note that the diode sensor used in this set-up had a stated dynamic range of - 20 to +20 dBm, compared to -30 dBm to +20 dBm for the thermal sensor. However, in our application the thermal sensor is being used to measure average power over a large time span including both on and off pulse conditions, whereas the diode sensor is used to measure the signal during a gated interval during the on time of the pulse, where more significant power levels are maintained. Accordingly, the diode sensor has a clear advantage for lower pulse ranges because the signal can be gated and it can be decided under which time period the power should be measured.

From Figure.4.9 it can be clearly observed that precision begins to deteriorate significantly for the thermal sensor as the pulsed power goes below about -5 dBm.

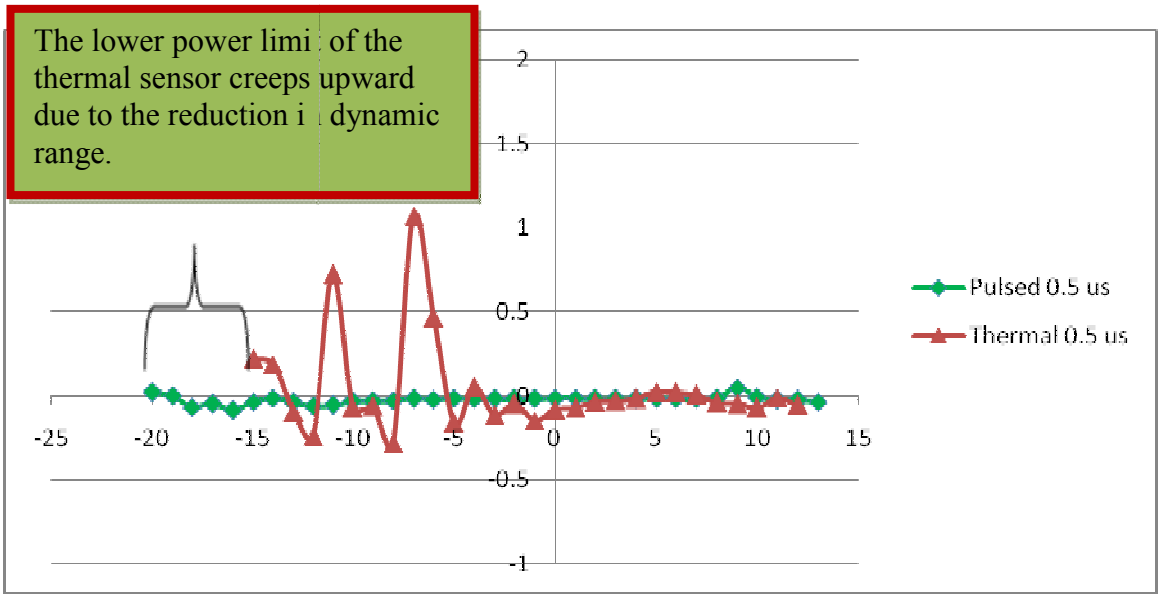


Figure.4.9. Thru Transducer Gain for the Diode and Thermal Sensors for τ = 0.5 µs, T = 100 µs (Duty Cycle = 0.5 Percent)

4.2. Measurement Results for Selected RF Power Transistors

Pulsed load-pull can be done by pulsing the RF input alone if the amplifier is operated in Class-B mode, since in Class-B mode the amplifier is turned ON only when RF input is ON. Even in low Class A/B mode we can get away with just pulsing the RF since even though the transistor's bias is static it is in the low region of the I(V) curve and the resulting self-heating will be very insignificant when compared to a Class A operation. For all the test results presented in this chapter, Class B operation was used.

4.3. Measurements on a Selected VDMOS Transistor

For doing pulsed measurements Maury has an option (as shown in Figure.4.10) where the user can enter the duty cycle of the waveform and this way Maury will automatically calculate the pulsed power. Pulsed load-pull was performed on a selected high power vertical MOS device using a time period 2ms and pulse width 200µs (Duty Cycle = 10%). After characterizing the system and tuners, a power calibration is done with a thru connection in place of the DUT.

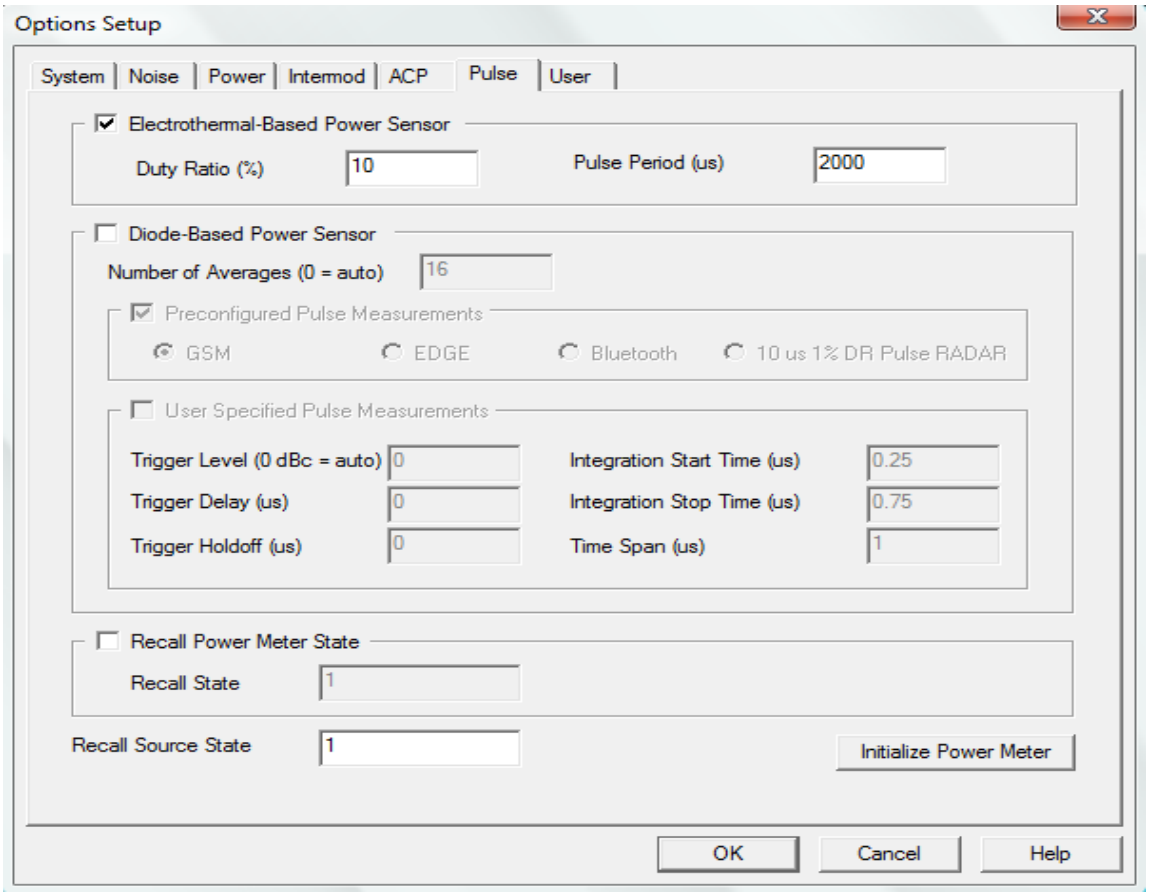


Figure.4.10. Pulsed Power Options in Maury v3

After calibrating the system for power, the DUT was measured and the results are shown below. There are two different ways to make a pulsed power measurement so to find the best way to do it three type of power sweeps were made with the DUT:

1) Swept power calibration with a CW input signal and then measure the 50 Ohm power sweep in the same CW mode
2) Swept power calibration with a CW input signal and then measure the 50 Ohm power sweep in pulsed condition
3) Swept power calibration with a pulsed signal and then do the 50 Ohm pulsed power sweep

   [Note: in all the pulsed condition shown below the time period was kept 2ms and pulse width was 100µs (Duty Cycle = 10%)]

   Figure.4.11. shows the variation in the Gt of the device

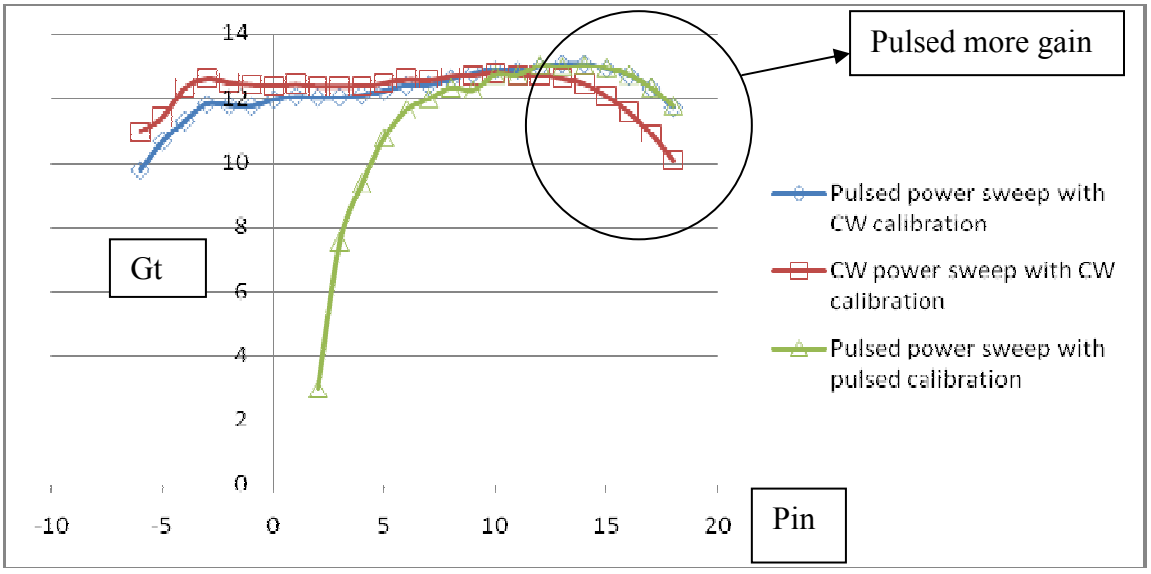


Figure4.11. Gain Gt of the Device at Various Conditions

From this plot it can be clearly seen that the pulsed signal gets more output power form the device as explained earlier. Also the red and blue curves are not together at lower input powers this is because at lower pulse width/input power as shown before in Figure.4.5 the pulse is not perfectly rectangular in shape and this causes inaccuracies in the thermal sensor. The next figure shows the Pin vs Pout for the DUT

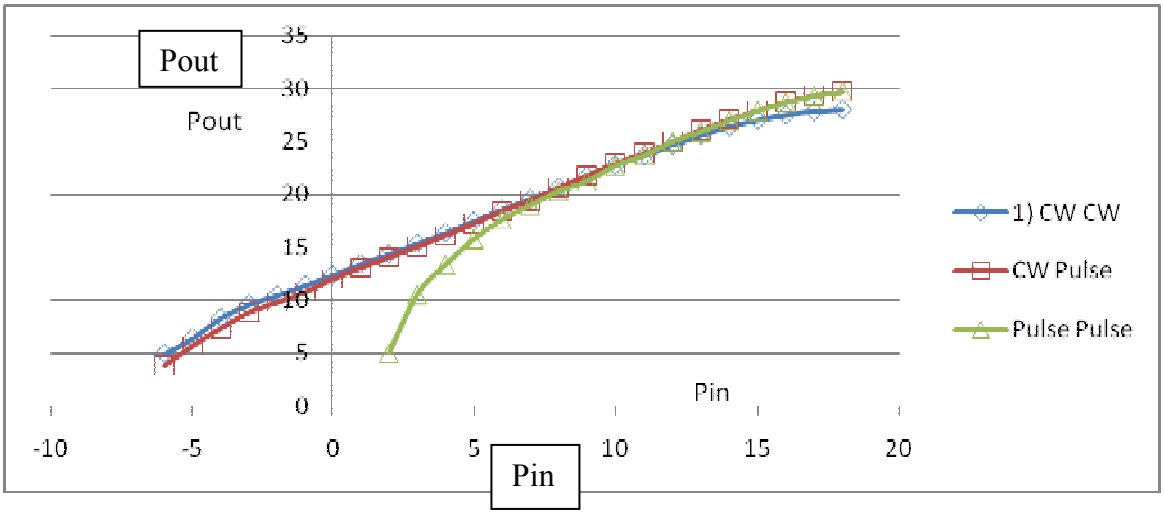


Figure.4.12. Pin Vs Pout for the DUT at Various Measurement Con litions

Even here it can be observed that the pulsed condition has more output power under large-signal drive. Figure.4.13 shows the efficiency measurement of the DUT at these conditions. But, as explained above when calculating efficiency using Maury software a correction has to be applied.

4.4. Efficiency Correction

The formula for efficiency as give in equation 3.6 is

$$\text{Efficiency} = 100 * \left(\frac{Pout - Pin}{Vout * Iout + Vin * Iin}\right)$$

In the above the input current *Iin* can be neglected for most FET devices; however, for pulsed operation, we need the correct *Iout* current in order to calculate the correct efficiency. This is because in the set-up we used a CW bias system which is only capable of measuring average current *Iavg*. So to calculate pulsed current *Iout* = *Ip* we use the formula shown below

$$Ip = \frac{(Iavg - Iq)}{DC} + Iq \qquad (4.1)$$

Where Iq is the quiescent current when the RF pulse is off, DC is the duty cycle of the RF pulse. Figure.4.14 shows an Ip representation.

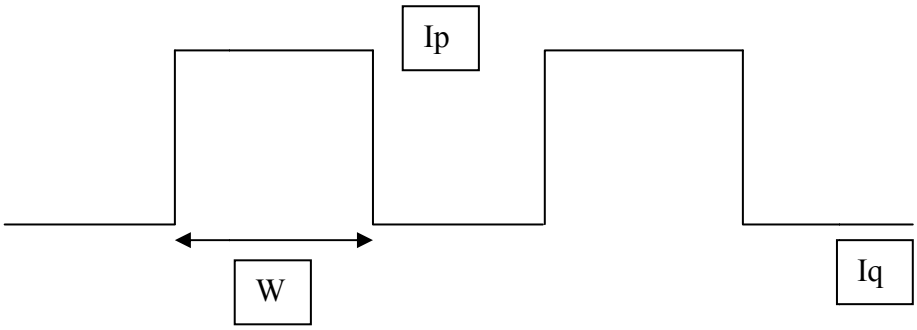


Figure.4.13. Ip Calculation for Efficiency

Once the correct Ip has been calculated corrected efficiency can be obtained. The corrected efficiency obtained by this method is shown is shown in Figure.4.14.

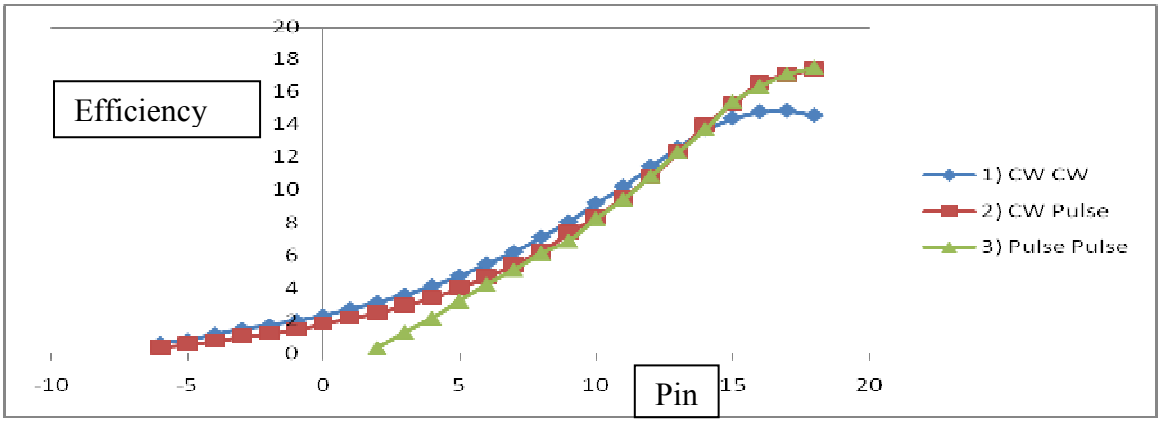


Figure.4.14. Efficiency of the Device at Various Measurement Conditions

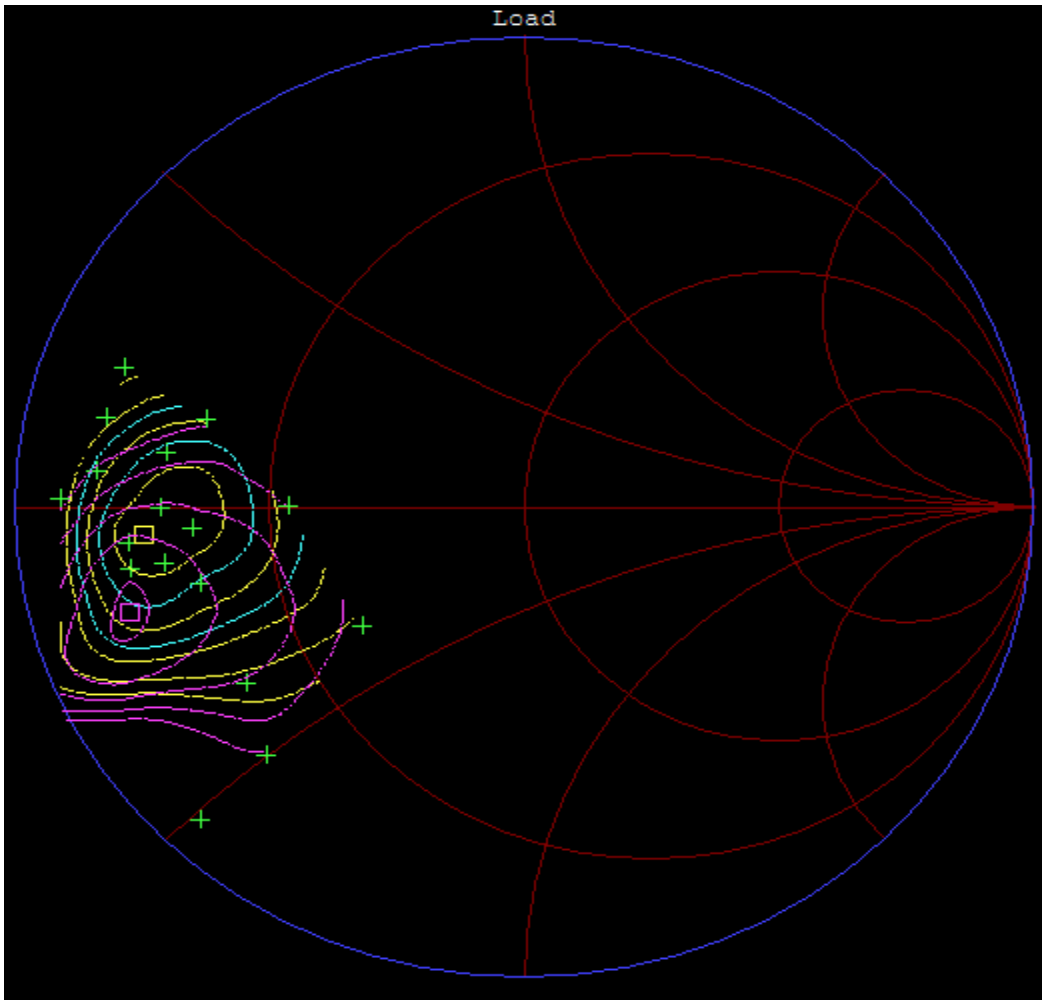
From all the three measurements shown above it can be seen that the pulsed power sweep with the CW calibration is the most favorable one. This is because when a pulsed calibration is done at 10% duty cycle using a thermal sensor the noise floor increases and the range of the sensor is reduced, and when a pulsed measurement is done with the same calibration the errors in the lower range gets carried over to the measurement but when a CW calibration is done the entire range of the sensor is calibrated; then when we do a pulsed measurement we have the entire range of the sensor even thought the lower power ranges might have some error. This explanation is clearly seen from the graphs shown above.

Table.4.1. Pulsed and CW load-pull comparison for different frequencies

Load-pull Condition	*Frequency Ghz*	*Pin dBm*	*Opt Load*	*Pout dBm*	*Gain dB*
CW	0.9	13	0.6416 < 149.27	32.24	19.24
Pulsed			0.6055 < 155.61	32.69	19.69
CW	1.2	17	0.7441 < -175.21	32.4	15.4
Pulsed			0.6506 < -177.18	33.26	16.26
CW	2.1	14	0.8032 < -80.06	29.46	15.46
Pulsed			0.7914 < -79.91	29.93	15.93

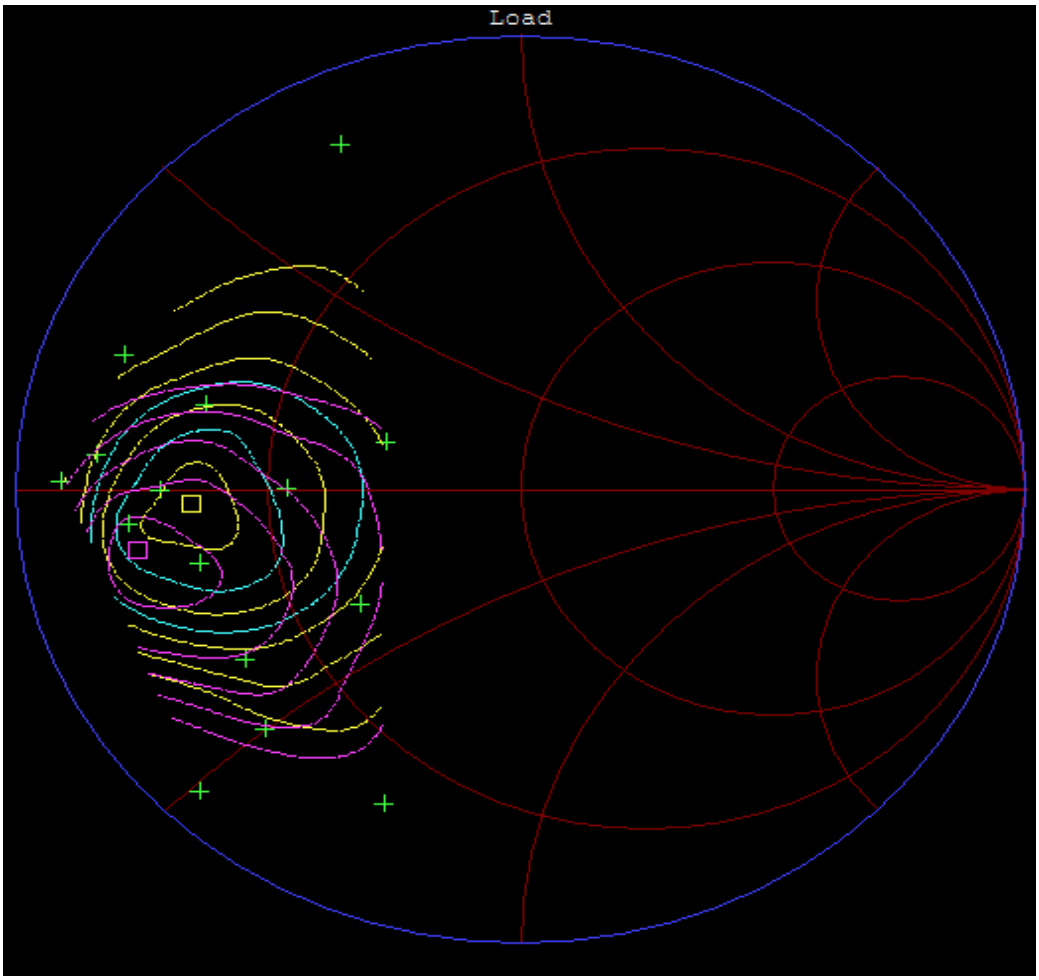
Following characterization and determination of the calibration type, the actual pulsed load-pull was done for the DUT. The pulsed load-pull measurements were done at three different frequencies 0.9GHz, 1.2 GHz and 2.1 GHz. Figure.4.15 and Figure.4.16 shows the CW and Pulsed load-pull performed respectively from these figures it can be seen that the pulsed load-pull has more gain and Pout. The Table.4.1 below shows the gain and Pout 1 dBm for the various frequencies. Even though the difference may not always be significant, the pulsed operation is safer for the device which will be explained in the later part.

From Figure.4.15 and Figure.4.16 it can be seen that the pulse and CW load-pull measurements have different optimum load impedance, as discussed in [19]. Also, pulsed load-pull has more gain and Pout when compared to CW measurement. Some experiments were done with the pulsed load-pull system where the time period was kept constant at 2 ms and the pulse width was varied between 200 µs and 400 µs for the variation of duty cycle from 10% to 20%. Figure.4.17 show that, as the duty cycle (pulse width) increases the device is pushed into more compression earlier.




```
Pout          max = 32.40 dBm
  at   0.7441<-175.21
 5  contours,  0.50 dBm step
(30.00 to 32.00 dBm)
Gt            max = 15.40 dB
  at   0.7441<-175.21
 5  contours,  1.00 dB step
(11.00 to 15.00 dB)
Gt(s)         max = 21.10 dB
  at   0.8043<-163.58
 5  contours,  1.00 dB step
(17.00 to 21.00 dB)
```

Figure.4.15. CW Load-pull




```
Pout          max = 33.26 dBm
  at   0.6506<-177.18
 5  contours,  0.50 dBm step
(31.00 to 33.00 dBm)
Gt            max = 16.26 dB
  at   0.6506<-177.18
 5  contours,  1.00 dB step
(12.00 to 16.00 dB)
Gt(s)         max = 20.41 dB
  at   0.7656<-169.88
 5  contours,  1.00 dB step
(16.00 to 20.00 dB)
```

Figure.4.16. Pulsed Load-pull with DC 10%

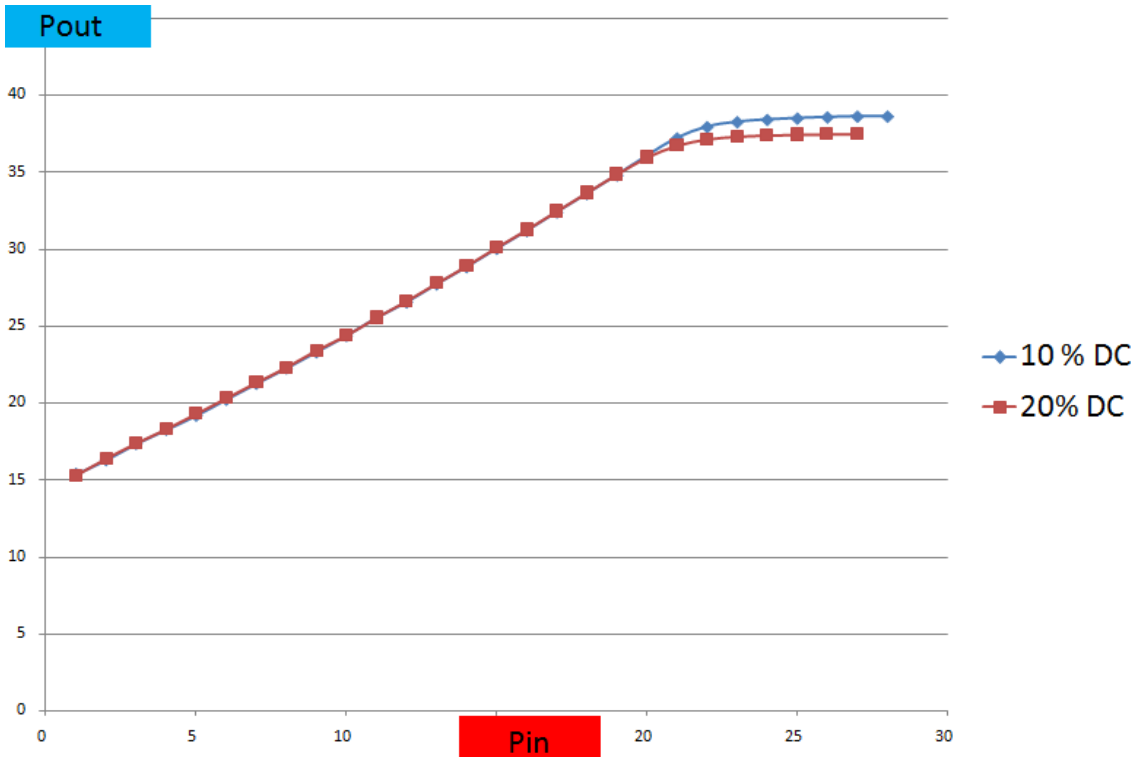


Figure.4.17. Power Sweep with Opt Load Γ for Max Power and Opt Source Γ for Gain

In Figure.4.18 it can be observed that the gain of the DUT has decreased and pushed into compression sooner. Figure.4.19 shows the efficiency plot (with corrected Iout for pulsed current) of the DUT for the same conditions and it can be seen that the efficiency is found compress at a higher rate for 20% when compared to 80% duty cycle due the self-heating and decrease in Pout.

These results show the importance of pulsed load-pull in testing the device in linear safe region.

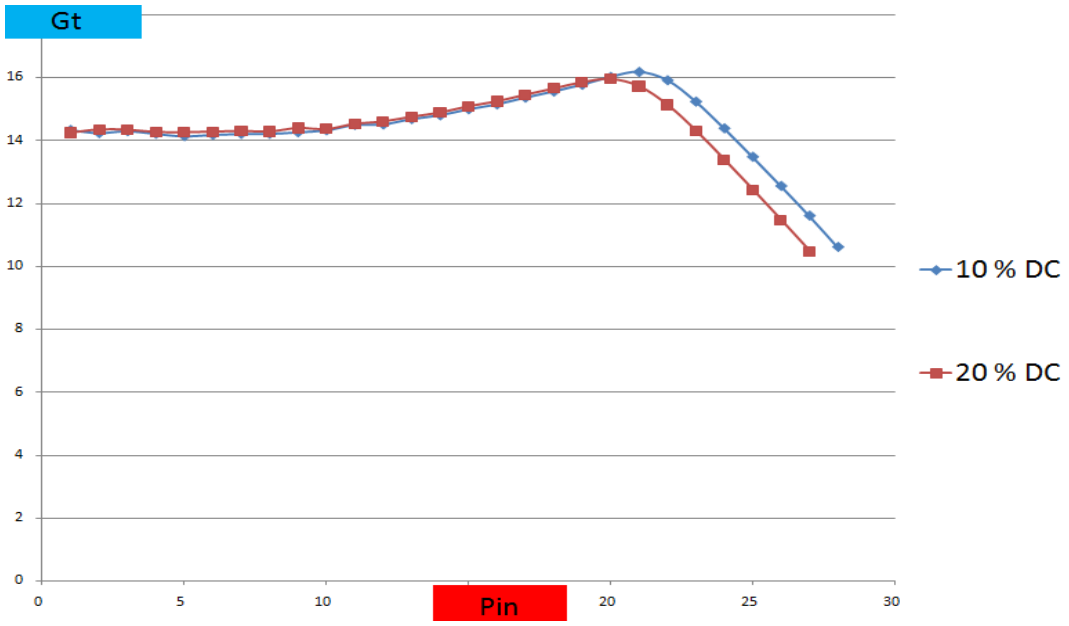


Figure.4.18. Gain Comparison for Different Pulse Width/ Duty Cycle

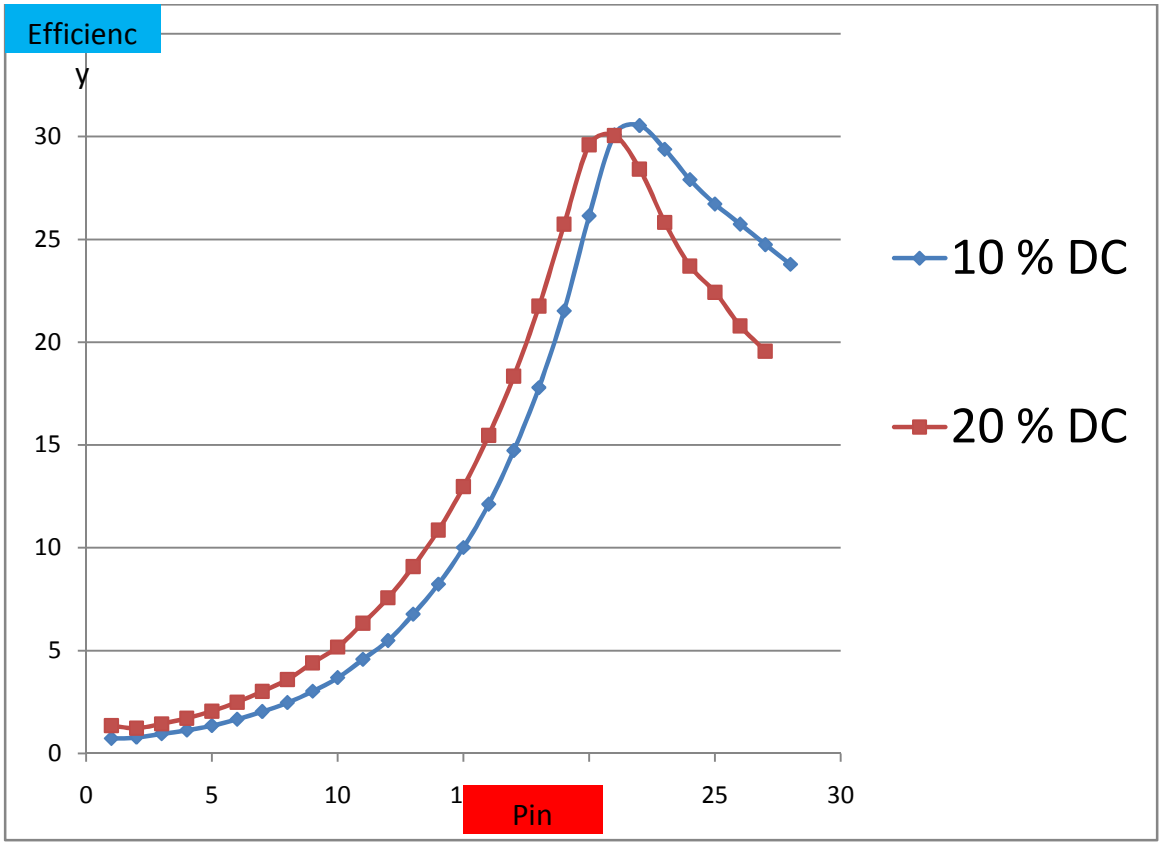


Figure.4.19. Efficiency Comparison for Different Pulsed Widths / Duty Cycles

4.5. Pulsed Load Pull for a Selected LDMOS Transistor

In this section pulsed load-pull is performed on a LDMOS 10 W transmission amplifier. The device was operated in class B condition so that it turns ON when the RF input is ON.

4.6. Measurement Results:

Figure.4.20 shows the Pin Vs Pout for various duty cycles form 10 µs (W = 10 µs and S = 100 µs) to CW. It can be clearly seen from the figures shown below that the device is affected by self heating.

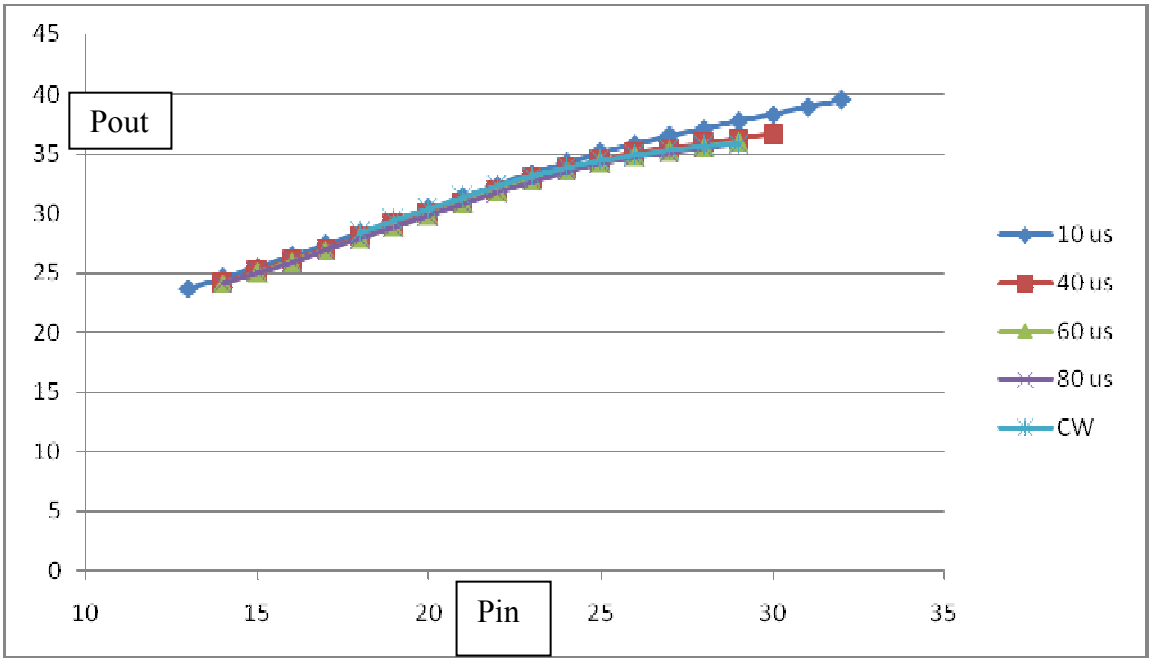


Figure.4.20. Pin Vs Pout for the LDMOS Transistor Under Various W with V_{gs} = 1.8 V and V_{ds} = 7.5 V

The device was pushed till 3 dB compression. But from Figure.4.20 it can be noted as the RF power is increased the device experiences more heating. Figure.4.21

shows the Pin Vs Gain c ırves for different *W*, even here it can be observed that the 10 µs *W* is not suffering from any self heating but as the *W* increase we can se ᵢ the decrease in gain. From Figure.4.22 t ıe difference in Efficiency (with corrected Iout) for the various *W* can be clearly seen.

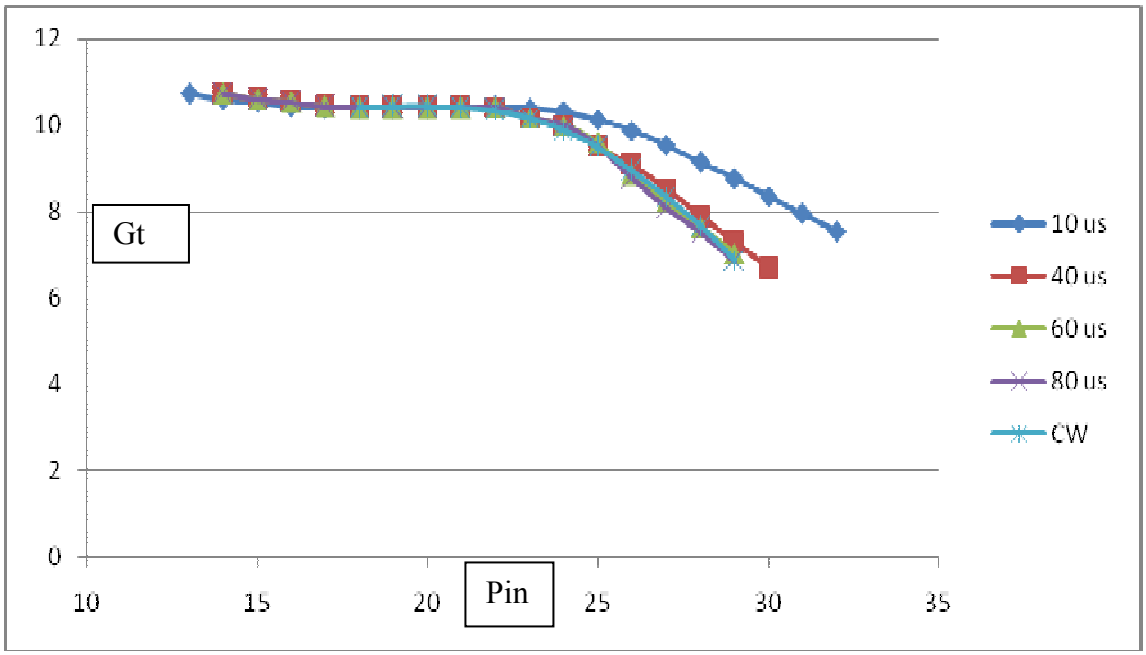


Figure.4.21. Pin Vs Gain for the LDMOS Transistor Under Various *W* with V_{gs} = 1.8 V and V_{ds} = 7.5 V

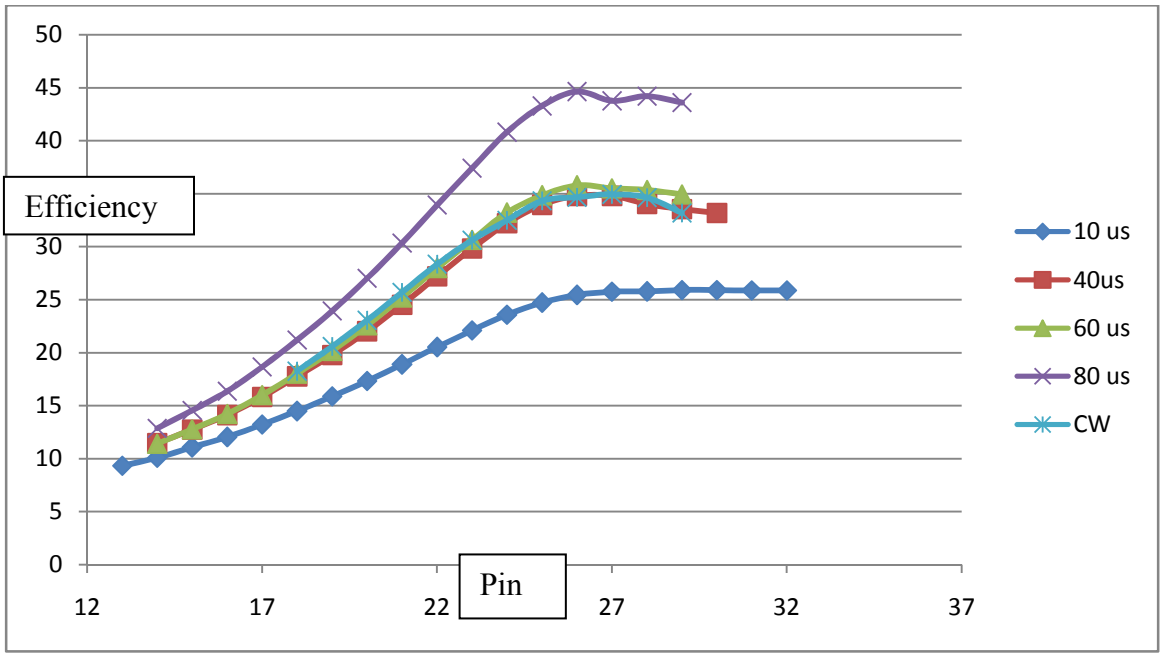


Figure.4.22. Pin Vs Efficiency for the LDMOS Transistor Under Various *W* with V_{gs} = 1.8 V and V_{ds} = 7.5 V

Also in the above figure it is evident that thought the efficiency is higher as we increase the *W* the efficiency compresses at a higher rate for larger *Ws.* It can be noted that for all the *W*s > 10 µs reach the 3 dB compression sooner than the 10 µs *W.*

The next figure shows the pulsed load-pull set-up used with the Minicircuits switch

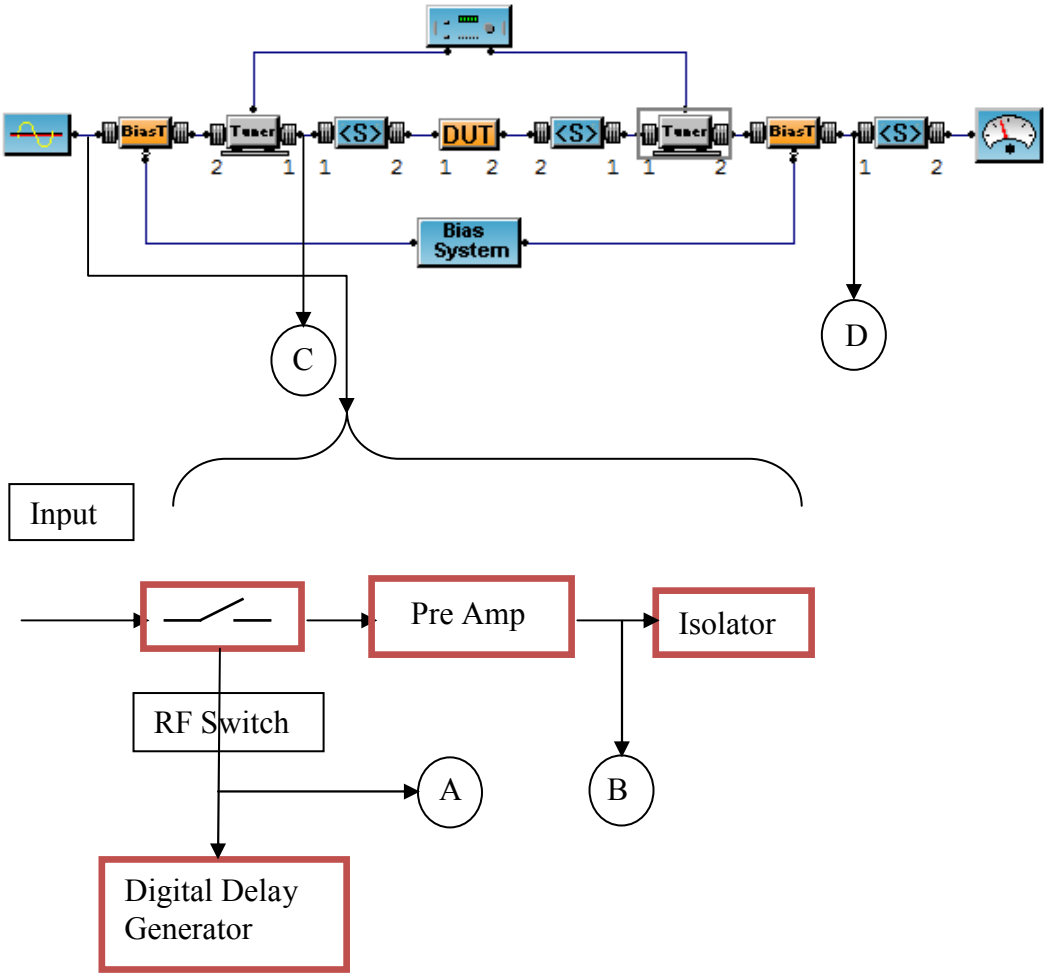


Figure.4.23. Pulsed Load-pull Set-up used for LDMOS Measurement with Labels Indicating the Different Points where the Oscilloscope Measurement was made.

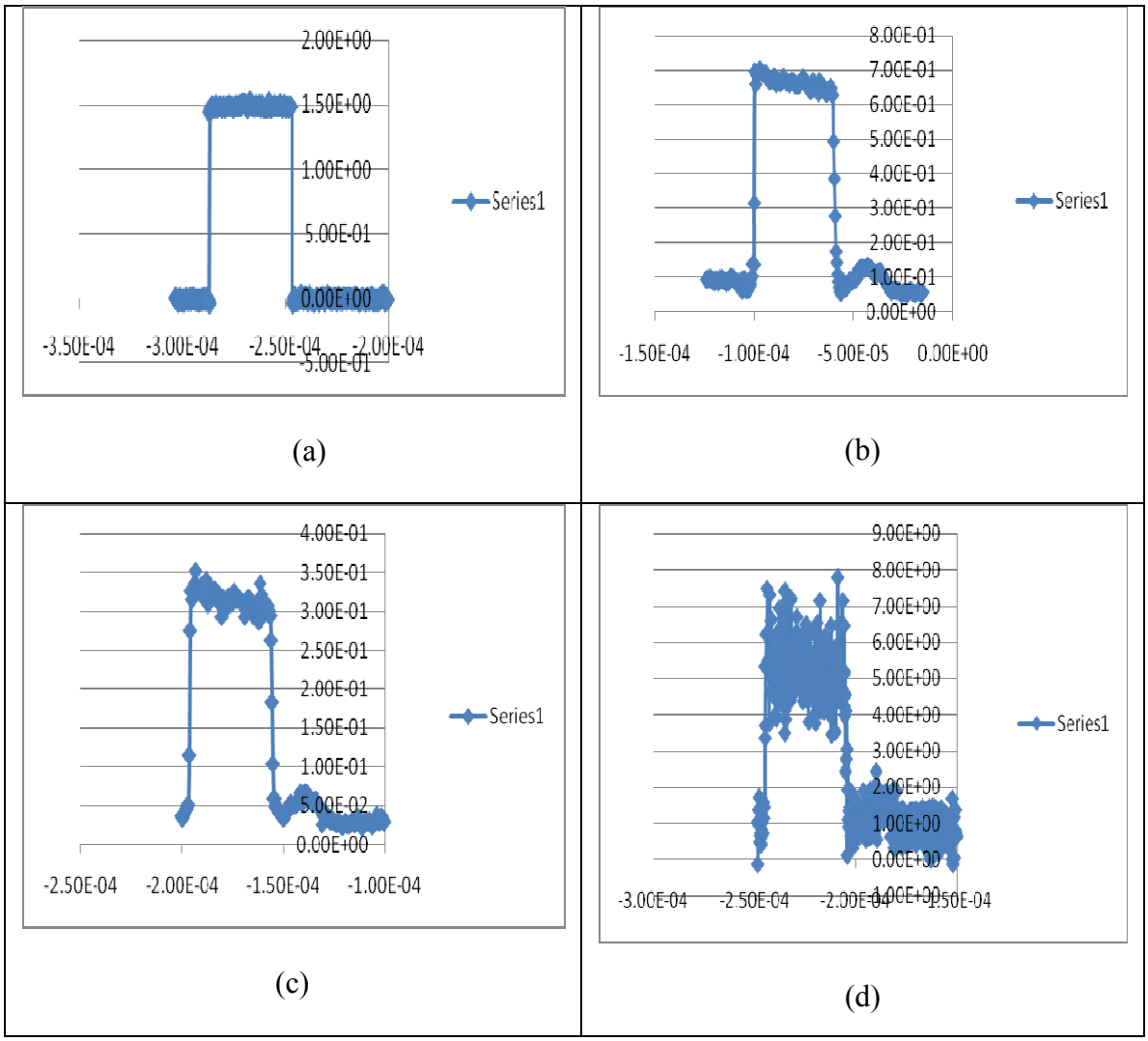


Figure.4.24. Oscilloscope Measurement at Different Points in the Pulsed Load-pull System for a *W* of 50 µs

From Figure.4.24 it can be noted that the pulsed signal is clean at the digital signal generator but as it passes through the switch and pre-amplifier more noise is added. The last figure in Figure.4.24 (d) shows the pulsed signal after amplification from the device.

4.7. Summary

In this chapter a simple benchmarking technique was explained to explore potential system limitations. Also the tradeoffs involved in choosing a thermal sensor over a diode sensor were shown. After gaining confidence with the power bench pulsed load-pull was done on VDMOS and LDMOS transistors. From the results shown it is evident that pulsed load-pull has more Pout and gain and less compression when compared to CW condition. Also since both the devices where operated in Class B condition the significant difference in Pout, Gain and Efficiency appear at high Pin where the bias of the device is also higher.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

This thesis has explored pulsed I (V) simulation technique to predict duty-cycle dependent self-heating has been demonstrated using a MET model for a power MOSFET. This simulation technique provides an additional reliable (and likely more convenient) method to extract the thermal time constant τ_{Th} by doing a curve fitting between the pulsed I(V) simulation of an electro-thermal non-linear model and the pulsed I(V) measured data with varied duty cycles. By using this simulation method, an custom transient measurement set-up to extract the thermal time constant can be avoided. Parameters for a three pole electro-thermal circuit was obtained and shown to have a better fit than a simple single-pole electro-thermal circuit for the MOSFET used in the experiments.

A secondary goal of the thesis was to explore pulsed load-pull measurements. As part of this, a thorough analysis of the pulsed power system was done. The results of an experiment to compare the accuracy and precision of pulsed power measurements using two different types of power sensors were shown. Pulsed power measurements for various duty cycles have been analyzed. As expected, the dynamic range of the thermal sensor used reduces as the duty cycle reduces, while the diode sensor set-up produced more accurate readings for lower duty cycle values. Limitations of the diode sensor to measure for low duty cycles at low power values were traced to limitations of the pulse

shape generated by the RF switch used. The benchmark methods outlined here shold prove helpful in developing confidence in a given test system, and provide insight on what duty cycles and power ranges can be used with confidence for testing of active devices.

In the final chapter pulsed load-pull results are presented. Testing was performed on example VDMOS and LDMOS transistors. Both these devices were operated in Class B operation ($V_g < V_{th}$). In this case, the device turns ON when the RF input in ON, i.e., the device bias is controlled by the RF signal. This is evident as in all Pin Vs Pout and Pin Vs Gain curves the increase in heating (decrease in Pout or Gain) is always at the high RF power region, which of course correspond to the highest current and highest thermal power dissipation. Careful attention to correcting the obtained efficiency data by estimating the peak current was important to obtaining efficiency data.

This work has given rise to several areas where further study. Following the modification in the MET model for self-heating more work can be done to show how to apply similar pulsed I(V) simulation techniques to address devices with trapping (eg., GaAS pHEMTs and GaN HEMTs). Pulsed load-pull developed by this work can be further advanced to measure devices in high class AB or class A bias condition by using a pulsed bias system which is synchronized with the pulsed RF source. Further pulsed load-pull simulation can be performed in ADS by using envelop simulation for suitable models.

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APPENDICES

Appendix A: Pulsed Bias Tee Measurements

In Chapter 4 the pulsed load-pull bench was discussed. In that chapter we saw how different components in the bench can cause errors in the pulsed power measurements. Bias tee form an important components of the pulsed power system i.e., the bias tee's DC path should allows bias pulses to pass through to the device unchanged, while still allowing RF measurements at as low a frequency as possible.

All the bias tees were tested under two pulsed conditions

(1) Pulse width 8 us and period 80 us (10% duty cycle)

(2) Pulse width 4 us and period 80 us (5% duty cycle). Digital Delay Generator was used to generate the pulses.

Figure.A.1 show the set-up used

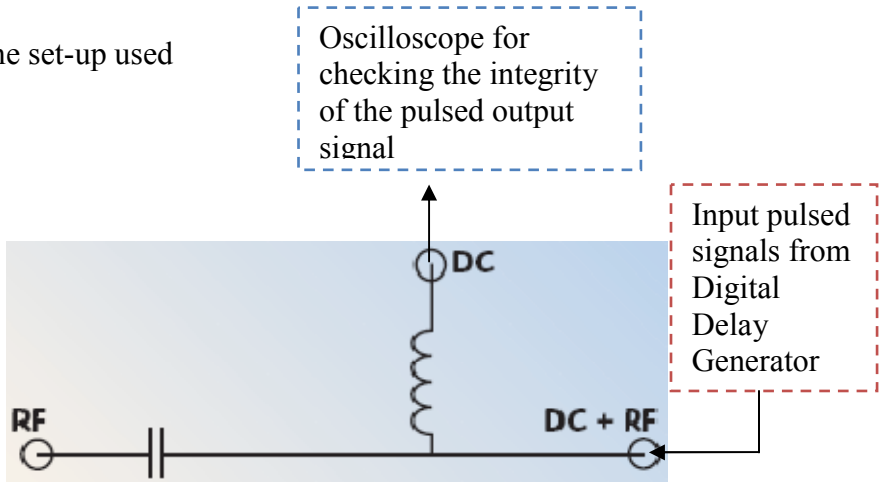

Figure.A.1. Bias Tee Measurement Set-up

The digital delay generator's pulse was used to give the pulsed signal needed to check the DC path of the bias tees. The results are shown below.

Appendix A (Continued)

Results:

Totally four bias tees were tested for the project

1) Picoseconds lab bias tee 5587

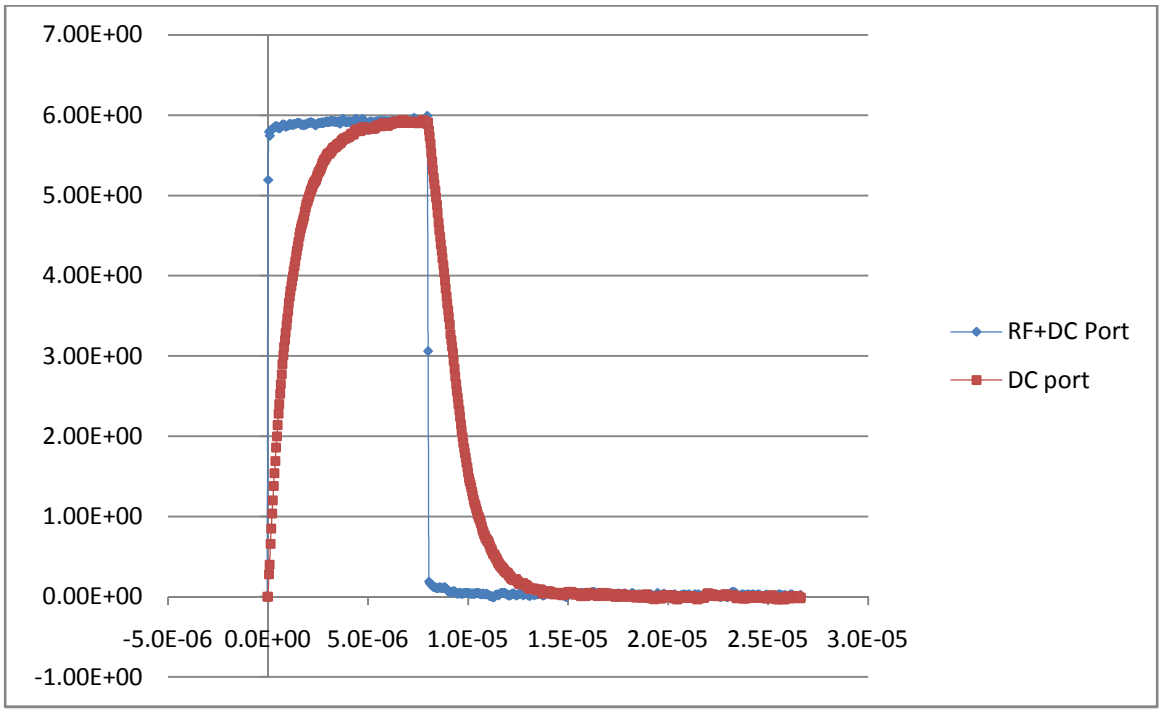

Figure.A.2. Pulse Width 8 µs and Period 80 µs (10% Duty Cycle for Picoseconds Lab Bias Tee 5587)

From the above figures it can be seen that the input and output pulses are almost equal in shape which indicates that this is a good bias tee for pulsed RF operations.

Appendix A (Continued)

2) Inmet Bias tee 8820SFF2-02

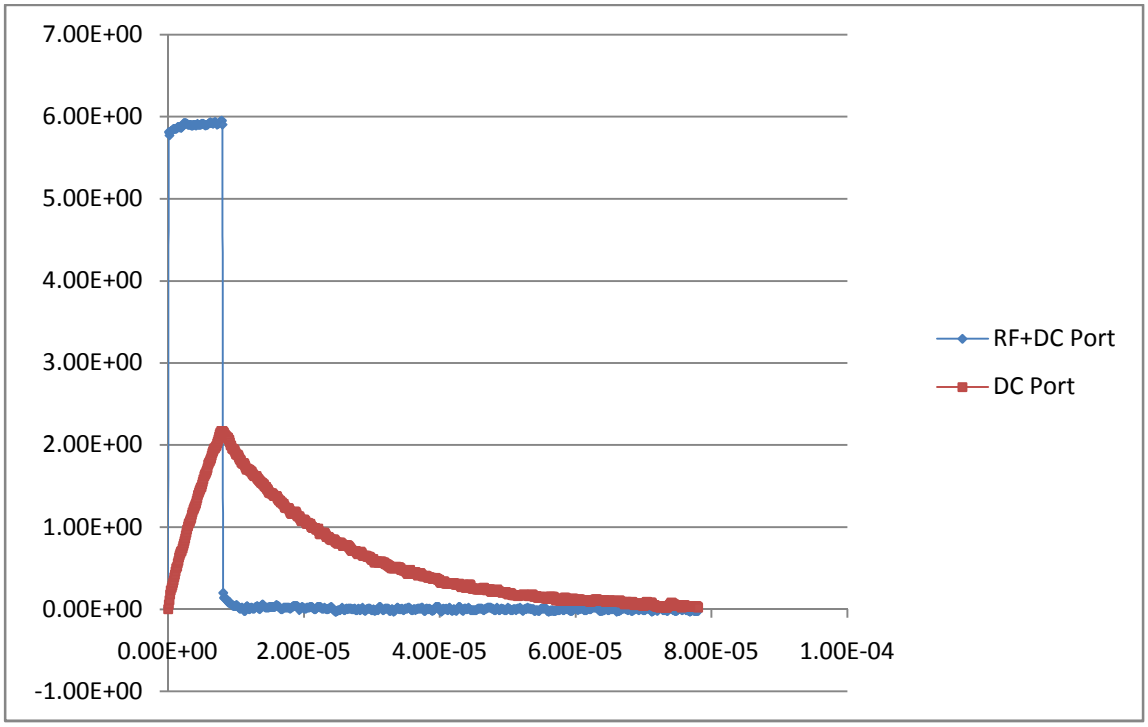

Figure.A.3. Pulse Width 8 us and Period 80 us (10% Duty Cycle for Inmet Bias Tee)

From the above figure it is apparent that this particular bias tee significantly distorts the pulsed signal and so this bias tee can be ruled out for pulsed bias set-ups with similar pulse widths.

Appendix A (Continued)

3) Minicircuits bias tee ZFBT-4RGW:

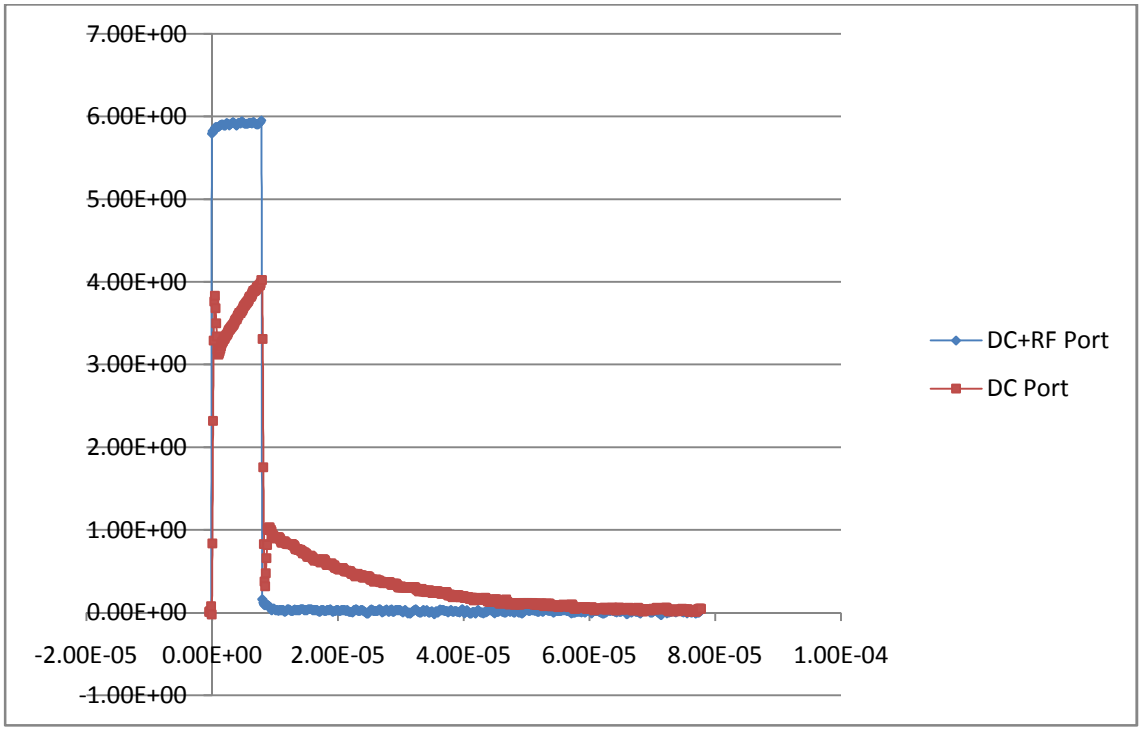

Figure.A.4. Pulse width 8 us and Period 80 us (10% Duty Cycle for Minicircuits Bias Tee ZFBT-4RGW)

From the above figure the Minicircuits bias tee does not preserve the integrity of the pulsed signal and so this bias tee can be ruled out for pulsed power set-ups.

4) Custom bias tee:

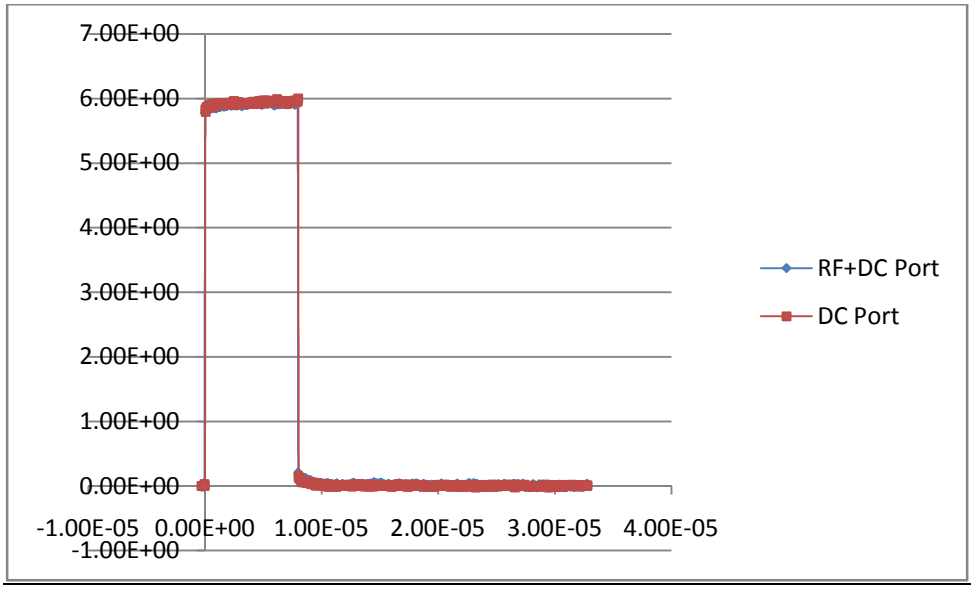

Figure.A.5. Pulse width 8 us and Period 80 us (10% Duty Cycle for Custom Bias Tee)

From the above figure this bias tee has a very good pulse performance since the output pulse is preserved, so with all the bias tees used to compare the last custom bias tee has the best performance.

Appendix B: R_{TH} Extraction

In Figure.2.1 the channel temperature at DC and low frequencies is related to the power dissipated in the channel by

$$T_c = R_{TH}P_d + T_a \qquad (B.1)$$

Pulsed I(V) was done with the lowest pulse width setting which was 0.2 µs using the Auriga Pulsed I/V system (the pulse width (0.2 µs), time period (0.5 µs) was kept constant, and the power dissipation value was changed to get the different curve) . NEC LDMOS device was chosen for this R_{TH} extraction experiment shown in Figure.B.1. The measurement required are listed below

1) Pulsed I(V) with zero power dissipation (Q point V_g = 0 V and V_d = 0 V), the temperature of the chuck was kept at 81°C. From literature we know that for pulsed I(V) with zero power dissipation the channel temperature is equal to the chuck temperature. So equation B.1 becomes

$$T_c = T_a\ (= 80) \qquad (B.2)$$

2) Now another pulsed I(V) was measured but this time with non zero power dissipation (Q point Vg = 2.1 V and Vd = 8V), now the chuck temperature was reduced to room temperature 25°C. Figure.B.2 shows the different power dissipation values of the pulsed I(V) curves obtained for extraction . At this Q point the power dissipation was 2.4 W. So equation B.1 becomes

$$T_c = R_{TH}*2.4 + 25 \qquad (B.3)$$

Appendix B (Continued)

3) Several pulsed I(V) measurements were made with different non zero power dissipations. A particular Vg curve was chosen from the pulsed I(V) curves, the non zero power dissipation curve which matched with the zero power dissipation curve was chosen to give the best fit.

4) So once a good match is obtained then we can equate B.2 and B.3 to get

$$81 = P_{diss} * R_{TH} + 25 \qquad \text{(B.4)}$$

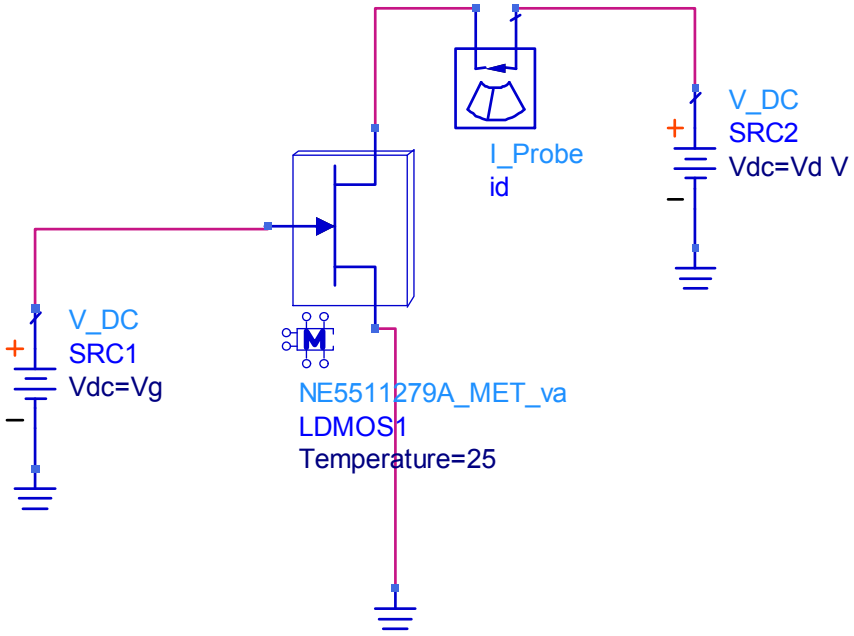

Figure.B.1. NEC LDMOS Model and Schematic used for R_{TH} Extraction

Appendix B (Continued)

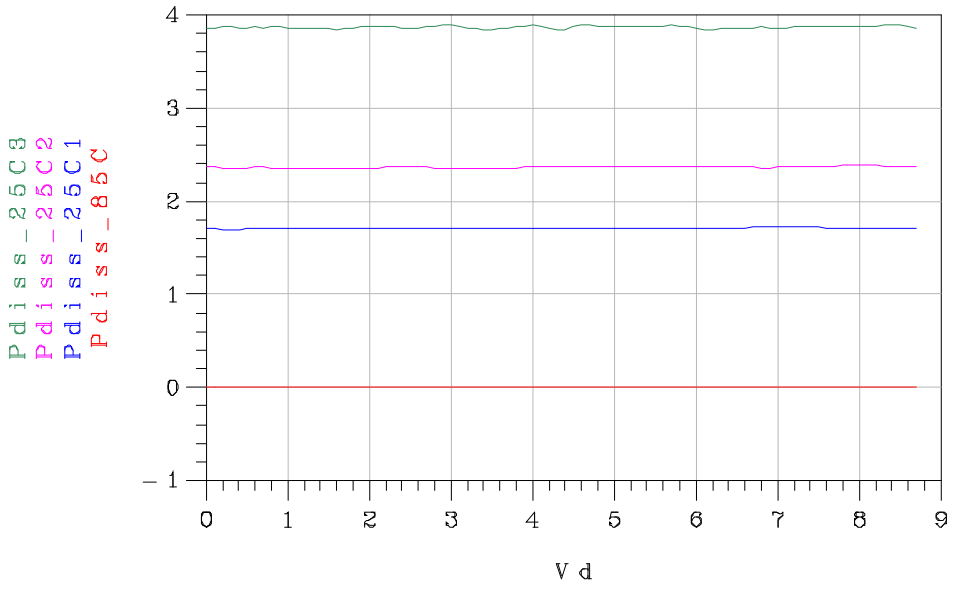

Figure.B.2. Power Dissipation for the Various Pulsed I(V) Curves.

From above figure it can be noted that we have one pulsed I(V) with zero power dissipation (red), and other curves with different power dissipations. From these I(V) curves a particular V_g curve was chosen for fitting and extracting R_{TH}. In this case V_g = 2.6 was selected.

Appendix B (Continued)

Figure.B.3 shows the fitting that was done to obtain the R_{TH} value

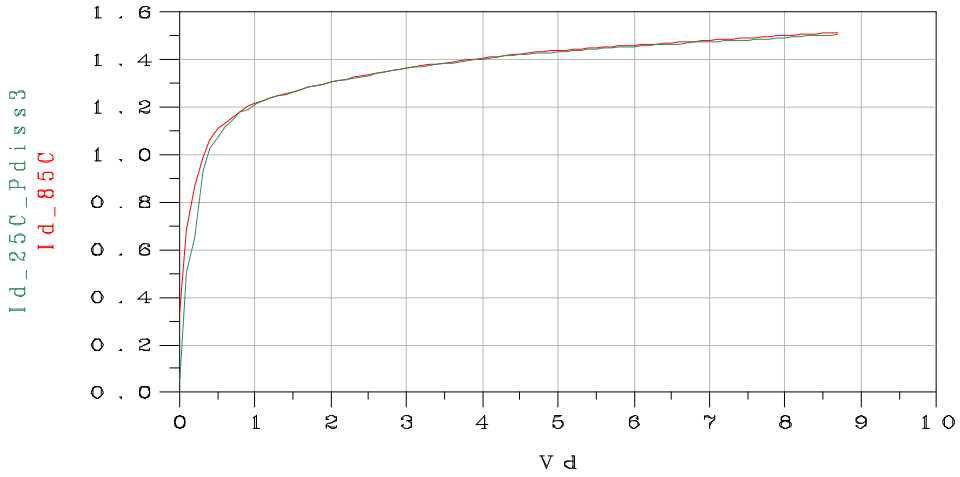

Figure.B.4. V_g = 2.6 V Curve for Red T_a = 81°C, Q Point V_d = 0 V, V_g = 0 V; Green T_a = 25°C, Q Point V_d = 12 V, V_g = 2.1 V

In the above figure the green curve had a power dissipation of 3.8 W. Now equation B.4 becomes

$$81 = 3.8 * R_{TH} + 25$$

$$\Rightarrow \quad R_{TH} = 14.74 \, ^\circ\frac{C}{W}$$